Very Short Answer Questions (PYQ)

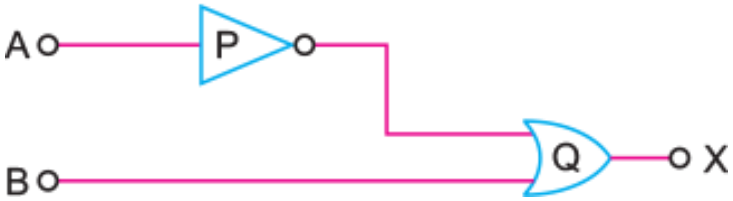
Q. 1. What happens to the width of depletion layer of a p-n junction when it is (i) forward biased, (ii) reverse biased? [CBSE Delhi 2011]

Ans. (i) When forward biased, the width of depletion layer decreases.

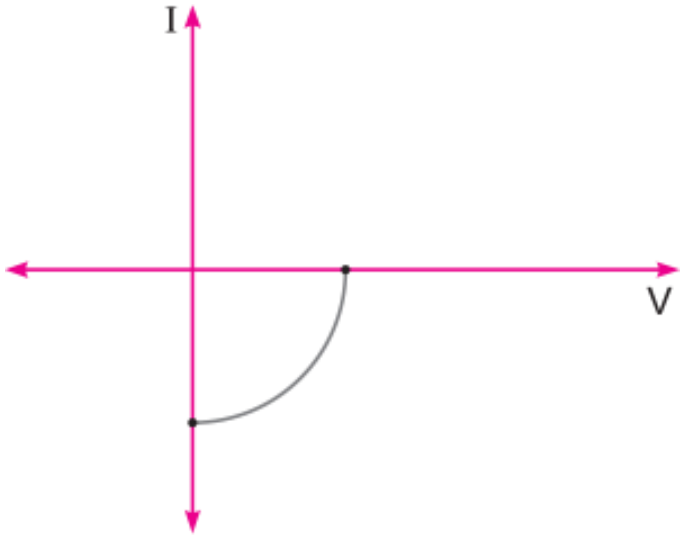
(ii) When reverse biased, the width of depletion layer increases.

Q. 2. Name the logic gates marked P and Q in the given logic circuit. [CBSE South 2016]

Ans. P is NOT gate and Q is OR gate.



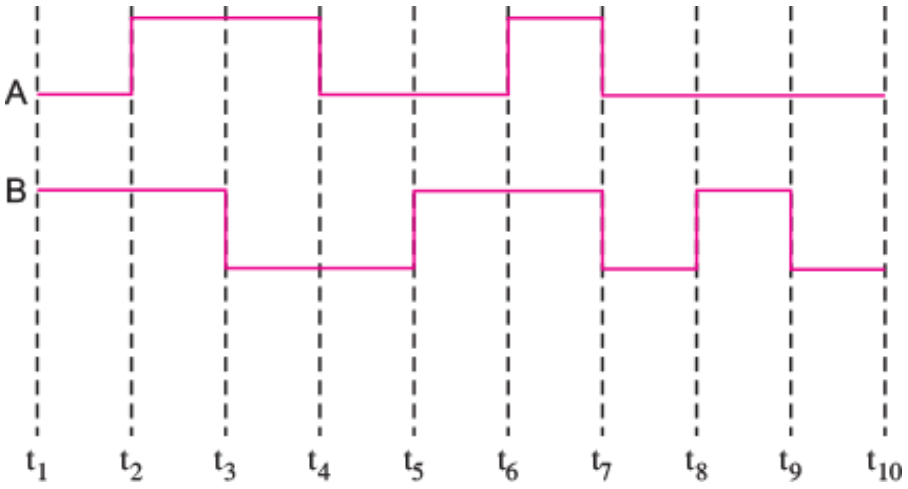
Q. 3. Name the junction diode whose I–V characteristics are drawn below: [CBSE Delhi 2017]



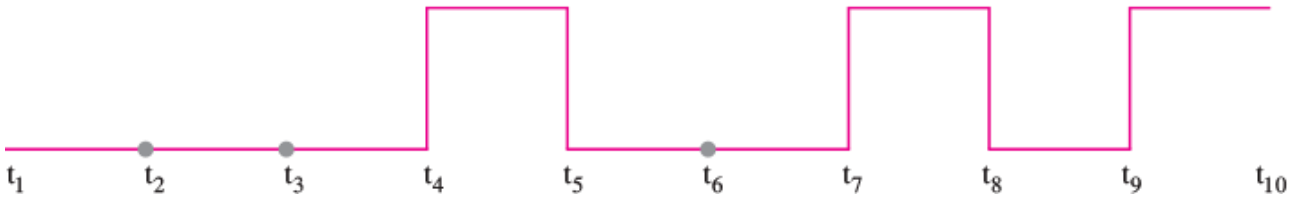
Ans. Solar cell

[**Note:** The I-V characteristics of solar cell is drawn in the fourth quadrant of the coordinate axis. This is because a solar cell does not draw current but supplies the same to the load.]

Q. 4. Two signals A and B are used as inputs of a NOR gate. Draw the output wave form. [CBSE East 2016]



Ans.



Q. 5. At what temperature would an intrinsic semiconductor behave like a perfect insulator? [CBSE Delhi 2009]

Ans. An intrinsic semiconductor behaves as a perfect insulator at temperature 0 K.

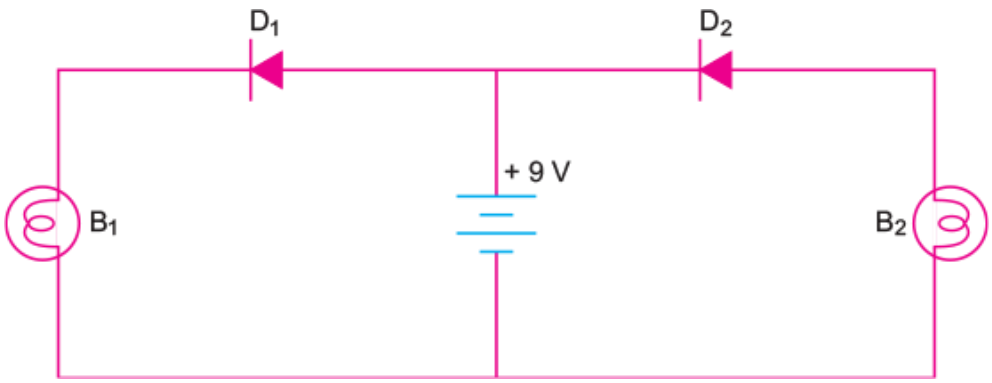
Q. 6. How does one understand the temperature dependence of resistivity of a semiconductor? [CBSE (F) 2010]

Ans. When temperature increases, covalent bonds of neighbouring atoms break and charge carrier become free to cause conduction, so resistivity of semi-conductor decreases with rise of temperature.

Q. 7. In a transistor, doping level in base is increased slightly. How will it affect (i) collector current and (ii) base current? [CBSE Delhi 2011]

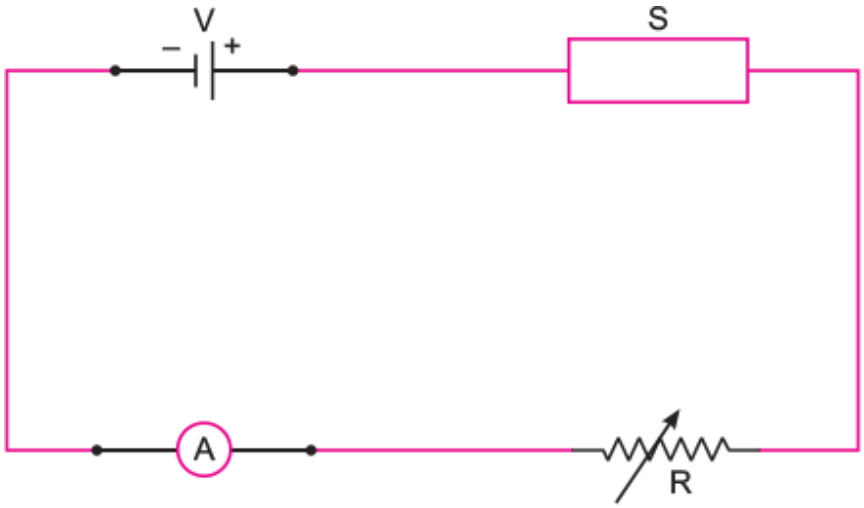
Ans. When doping level in base is increased slightly, (i) collector current decreases slightly and (ii) base current increases slightly.

Q. 8. In the following diagram, which bulb out of B_1 and B_2 will glow and why? [CBSE (AI) 2017]



Ans. Bulb B_1 will glow as diode D_1 is forward biased.

Q. 9. In the following diagram 'S' is a semiconductor. Would you increase or decrease the value of R to keep the reading of the ammeter A constant when S is heated? Give reason for your answer. [CBSE (AI) 2017]



Ans. The value of R would be increased. On heating, the resistance of semiconductor (S) decreases.

Q. 10. What happens when a forward bias is applied to a p-n junction? [CBSE Panchkula 2015]

Ans. The direction of the applied voltage (V) is opposite to the built-in potential V_0. As a result, depletion layer width decreases and the barrier height is reduced to $V_0 - V$.

Very Short Answer Questions (OIQ)

Q. 1. Name two semiconductor materials.

Ans. Germanium, silicon

Q. 2. Name charge carriers in p-type semiconductor.

Ans. Holes

Q. 3. Name charge carriers in n-type semiconductor.

Ans. Free electrons.

Q. 4. If ni is density of intrinsic charge carriers; n_h and n_e are densities of hole and electrons in extrinsic semiconductor, what is the relation among them?

Ans. $n_e n_h = n_i^2$

Q. 5. Name fundamental logic gates.

Ans. OR, AND and NOT gates.

Q. 6. What is the approximate width of depletion layer in p-n junction diode?

Ans. The depletion layer in junction diode is of the order of micrometer (≈ 10^{-6} m).

Q. 7. What is the net charge on a given piece of (i) p-type semiconductor (ii) n-type semiconductor?

Ans. (i) Zero

(ii) Zero.

Q. 8. Name the type of charge carriers in p-n junction diode when forward biased.

Ans. Majority charge carriers: electrons and holes.

Q. 9. Name the type of charge carriers in p-n junction when reverse biased.

Ans. Minority charge carriers: electrons and holes.

Q. 10. What are charge carriers in p-n-p transistor?

Ans. Holes are charge carriers in p-n-p transistor.

Q. 11. What are charge carriers in n-p-n transistor?

Ans. Electrons are charge carriers in n-p-n transistor.

Q. 12. Which device is used as a voltage regulator?

Ans. Zener diode is used as a voltage regulator.

Q. 13. In a transistor, both emitter and collector regions are of the same nature of doping. Can these regions be interchanged?

Ans. No, the emitter and collector regions cannot be interchanged. Since these are differently doped.

Q. 14. Can we measure the potential difference across an unbiased p–n junction by connecting a sensitive voltmeter across it?

Ans. No, the reason is there are no free charge carriers in the depletion region. Hence, in the absence of any external battery, there is no current flowing through the junction.

Q. 15. What signal voltage is represented for positive logic state 1?

Ans. Positive logic state 1, represents signal voltage of +5V.

Q. 16. In the given logic circuit, name the logic gates 1 and 2 and write the name of the combination of gates.

Ans. Logic gate '1' is OR gate and logic gate 2 is NOT gate. The combination of gates is **NOR** gate.

Q. 17. Name the logic gate whose repetitive use can make digital circuits.

Ans. The repeated use of NAND or NOR gates alone can give all basic gates.

Q. 18. What is the frequency of output signal of (i) Half wave rectifier (ii) Full wave rectifier, if the frequency of input signal is 50 Hz?

Ans. For half wave rectifier, the output frequency = 50 Hz.

For full wave rectifier, the output frequency is 100 Hz.

Q. 19. What is the order of energy gap in a semiconductor?

Ans. The energy gap in a semiconductor is of the order of 1 eV.

Q. 20. How does the energy gap in a semiconductor vary, when doped with a pentavalent impurity?

Ans. The energy gap decreases.

Q. 21. How does the conductivity of a semiconductor change with rise in temperature?

Ans. The conductivity of a semiconductor increases with increase of temperature.

Q. 22. What type of extrinsic semiconductor is formed when

(i) Germanium is doped with indium?

(ii) Silicon is doped with bismuth?

Ans. (i) Indium is trivalent, so germanium doped with indium is an p-type semiconductor.

(ii) Bismuth is pentavalent, so silicon doped with bismuth is a n-type semiconductor.

Q. 23. How is a sample of an n-type semiconductor electrically neutral though it has an excess of negative charge carriers?

Ans. The sample contains atoms of either original material or the impurity which are all neutral.

Q. 24. Give the ratio of number of holes and number of conduction electrons in an intrinsic semiconductor.

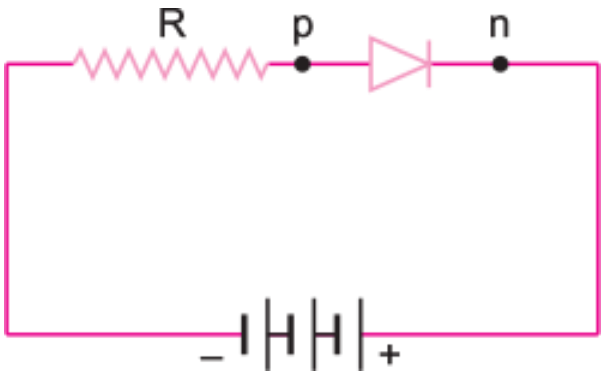
Ans. Ratio = 1: 1.

Q. 25. In a semiconductor the concentration of electrons is 8×10^{13} cm^{-3} and that of holes is 5×10^{12} cm^{-3}. Is it a p-type or n-type semiconductor?

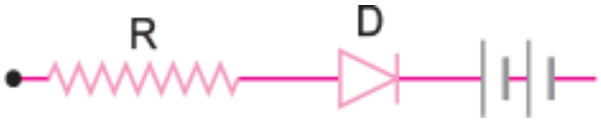
Ans. As concentration of electrons is more than the concentration of holes, the given extrinsic semiconductor is n-type.

Q. 26. Draw a p-n junction which is reverse biased.

Ans. The p-n junction with reverse bias is shown in figure.



Q. 27. In the given diagram, is the diode D forward or reverse biased?



Ans. The given diode is reverse biased.

Q. 28. What is the value of electrical conductivity of a semiconductor at absolute zero?

Ans. At absolute zero, a semiconductor has no free charge carrier; hence the electrical conductivity of a semiconductor at absolute zero is **zero.**

Q. 29. State with reason why a photodiode is usually operated at a reverse bias.

Ans. The fractional change due to incident light on minority charge carriers in reverse bias is much more than that over the majority charge carriers in forward bias. This charge in reverse bias current is more easily measurable. So, photodiodes are used to measure the intensity in reverse bias condition.

Q. 30. State the factor, which controls (i) wavelength of light and (ii) intensity of light, emitted by a LED.

Ans. (i) Wavelength of light emitted depends on its band energy gap.

(ii) Intensity of light emitted depends on the forward current conducted by the p–n junction.

Q. 31. The energy gaps in the energy band diagrams of a conductor, semiconductor and insulator are E_1, E_2 and E_3. Arrange them in increasing order.

Ans. The energy gap in a conductor is zero, in a semiconductor is ≈ 1 *eV* and in an insulator is ≥ 3 *eV*.

∴ E_1=0, E_2 =1eV, E_3 ≥ 3*eV*

∴ $E_1 < E_2 < E_3$

Q. 32. State the reason, why GaAs is most commonly used in making a solar cell.

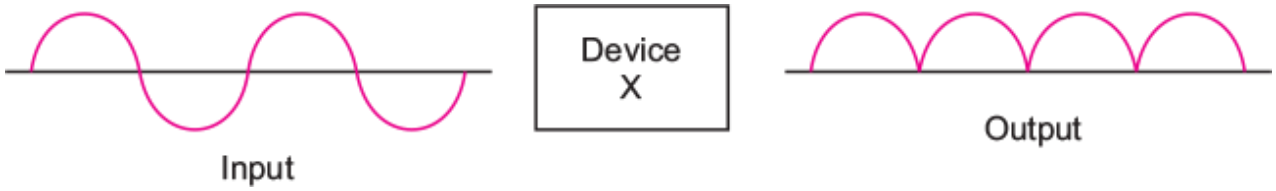
Ans. For solar cell, incident photon energy must be greater than band gap energy, *i.e*, (*hv* > *Eg*) For GaAs, *Eg*=1.43 *eV* = 1.43 eV and high optical absorption ≈ 104 cm^{-1}, which are main criteria for fabrication of solar cells.

Q. 33. Define trans conductance of a transistor.

Ans. The trans conductance of a transistor is defined as the ratio of the change in collector current to the change in base voltage at constant collector voltage.

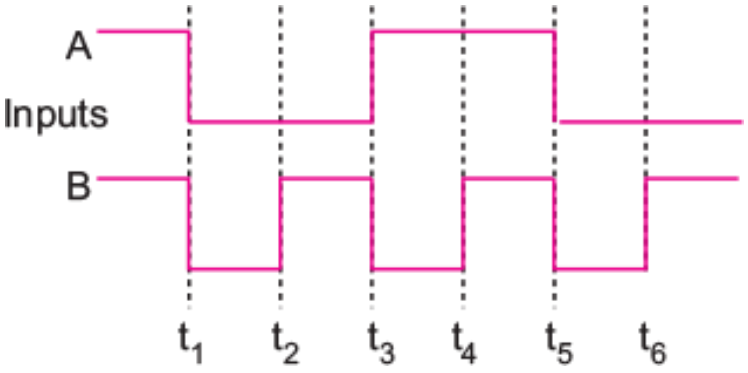
$$g_m = \left(\frac{\Delta I_C}{\Delta V_b}\right)_{V_C=\text{cons tan } t}$$

Q. 34. 'Device X' shown here, converts the input voltage waveform into the output voltage waveform as shown in fig. Name the device X.

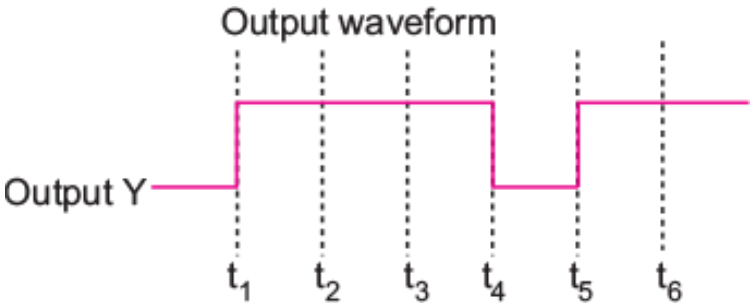


Ans. The box contains the circuit of full wave rectifier.

Q. 35. The given inputs A and B are fed to 2-inputs NAND gate. Draw the output waveform of the gate.



Ans. The output waveform is as shown



Q. 36. Why are elemental dopants for Silicon or Germanium usually chosen from group 13 or group 15? [HOTS][NCERT Exemplar]

Ans. The size of dopant atoms should be such as not to distort the pure semiconductor lattice structure and yet easily contribute a charge carrier on forming co-valent bonds with Si or Ge.

Q. 37. Sn, C, Si and Ge are all group 14 elements. Yet, Sn is a conductor, C is an insulator while Si and Ge are semiconductors. Why? [HOTS] [NCERT Exemplar]

Ans. If the valance and conduction bands overlap (no energy gap), the substance is referred as a conductor. For insulator the energy gap is large and for semiconductor the energy gap is moderate. The energy gap for Sn is 0 eV, for C is 5.4 eV, for Si is 1.1 eV and for Ge is 0.7 eV. Accordingly, their electrical conductivity varies.

Q. 38. Can the potential barrier across a p-n junction be measured by simply connecting a voltmeter across the junction? [HOTS] [NCERT Exemplar]

Ans. No, because the voltmeter must have a resistance very high compared to the junction resistance, the latter being nearly infinite.

Q. 39. In a CE transistor amplifier there is a current and voltage gain associated with the circuit. In other words there is a power gain. Considering power a

measure of energy, does the circuit violate conservation of energy? [HOTS] [NCERT Exemplar]

Ans. No, the extra power required for amplified output is obtained from the DC source.

Q. 40. Explain why elemental semiconductor cannot be used to make visible LEDs.
[HOTS] [NCERT Exemplar]

Ans. Elemental semiconductor's band-gap is such that electromagnetic emissions are in infrared region.

Short Answer Questions – I (PYQ)

Q. 1. Distinguish between a metal and an insulator on the basis of energy band diagrams. [CBSE (F) 2014]

Ans.

	Metal	**Insulators**
(i)	Conduction band and valence band overlap each other.	There is large energy gap between conduction band and valence band.
(ii)	Conduction band is partially filled and valence band is partially empty.	Conduction band is empty. This is because no electrons can be excited to it from valence band.

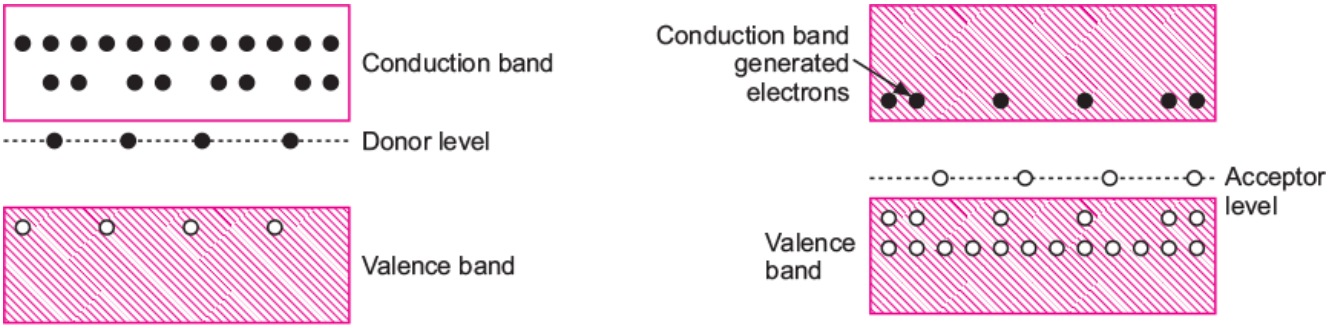
Q. 2. Write two characteristic features to distinguish between n-type and p-type semiconductors. [CBSE (F) 2012]

Ans.

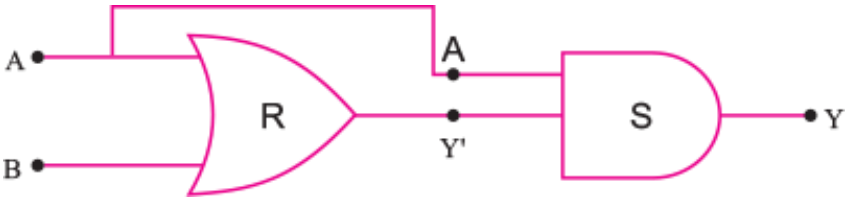
	n-type Semiconductor	**p-type Semiconductor**
(i)	It is formed by doping pentavalent impurities.	It is doped with trivalent impurities.
(ii)	The electrons are majority carriers and holes are minority carriers ($n_e >> n_h$).	The holes are majority carriers and electrons are minority carriers ($n_h >> n_e$).

Q. 3. Draw energy band diagrams of an n-type and p-type semiconductor at temperature T > 0 K. Mark the donor and acceptor energy levels with their energies.
[CBSE (F) 2014]

Ans.



Q. 4. Write the truth table for the combination of the gates shown. Name the gates used. [CBSE Delhi 2014]



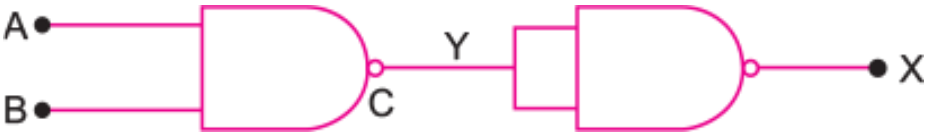
Ans.

Input		Y'	Y
A	B		
0	0	0	0
1	0	1	1
0	1	1	0
1	1	1	1

Gate R — OR gate

Gate S — AND gate

Q. 5. Draw the output waveform at X, using the given inputs A, B for the logic circuit shown alongside. Also identify the gate. [CBSE Delhi 2011]



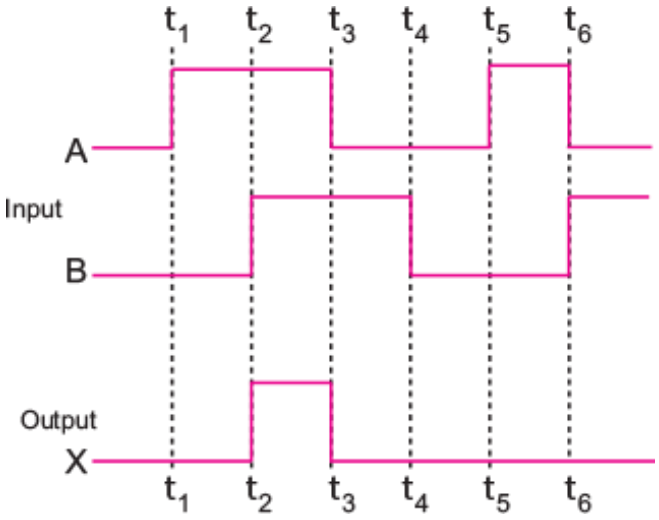
Ans.

$Y = A \,.\, \overline{B}$

and $X = \overline{Y} = A \,.\, B$

This is AND operation. Therefore, the output is 1 when both inputs are 1.

Accordingly the waveform output is shown in figure.



Q. 6. Identify the logic gates marked P and Q in the given logic circuit. Write the truth table for the combination. [CBSE Delhi 2014]

Ans. P is 'NAND' gate and Q is 'OR' gate.

Truth Table

Input		Output
A	B	X
0	0	1
1	0	1
0	1	1
1	1	1

Q. 7. How is forward biasing different from reverse biasing in a p-n junction diode?
[CBSE Delhi 2011]

Ans. (1) Forward Bias:

(i) Within the junction diode the direction of applied voltage is opposite to that of built-in potential.

(ii) The current is due to diffusion of majority charge carriers through the junction and is of the order of mill amperes.

(iii) The diode offers very small resistance in the forward bias.

(2) Reverse Bias:

(i) The direction of applied voltage and barrier potential is same.

(ii) The current is due to leakage of minority charge carriers through the junction and is very small of the order of

(iii) The diode offers very large resistance in reverse bias.

Q. 8. The output of a 2-input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table.
[CBSE Delhi 2009]

Ans. Name of combination: NAND gate logic symbol.

Truth Table of NAND gate is

Input		Output
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

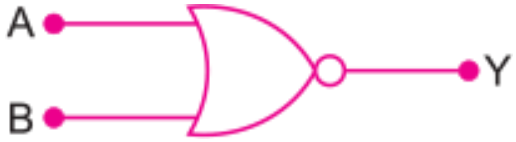
Q. 9. Draw the logic symbol of the gate whose truth table is given below:

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If this logic gate is connected to NOT gate, what will be output when (i) A = 0, B = 0 and

(ii) A = 1, B = 1? Draw the logic symbol of the combination. [CBSE (F) 2009]

Ans. The given truth table is of NOR gate. The logic symbol is shown in fig.

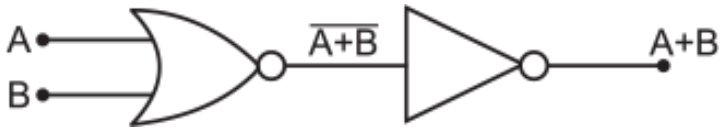


When it is connected to a NOT gate, the gate becomes OR gate.

(i) A = 0, B= 0 gives output 0.

(ii) A = 1, B = 1 gives output 1.

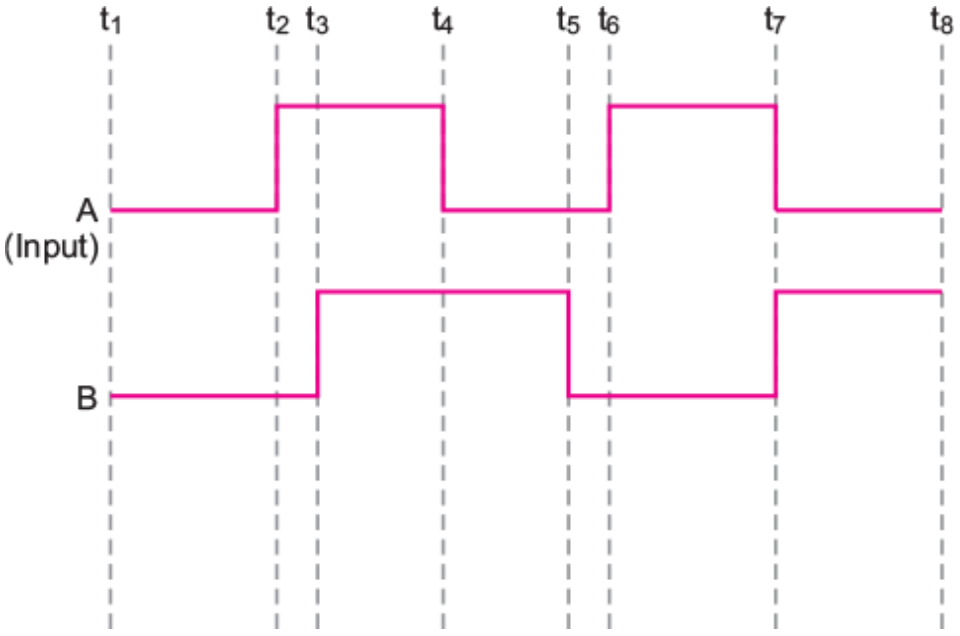
The combination is shown in fig.



Q. 10. Answer the following question :

(i) Identify the gate equivalent to the 'dotted box' shown here and give its symbol and truth table. [CBSE (AI) 2013, 2012, 2011, CBSE (F) 2014, 2010]

(ii) The input 'A' shown here is used with another unknown input 'B' in this set-up. If the output 'Y' has the form shown, give the intervals over which the input 'B' is in its 'high' state.



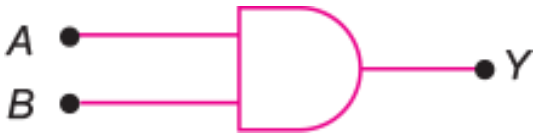
Ans. (i)

The output $Y = \bar{A} + \bar{B} = \bar{\bar{A}} \cdot \bar{\bar{B}} = AB$

That is equivalent gate is '**AND**' gate.

The symbol and truth table are shown in fig.

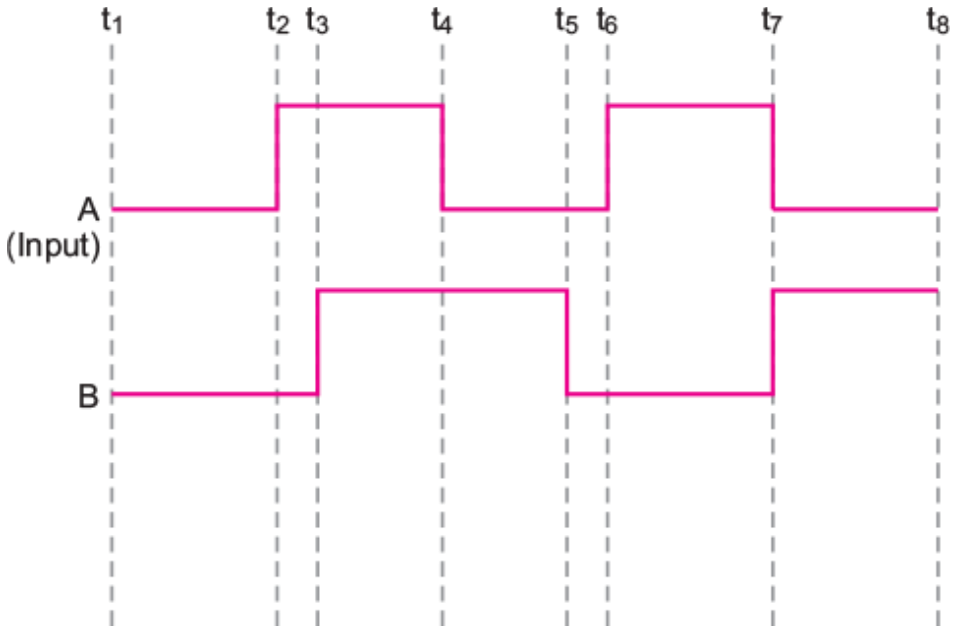
Truth Table



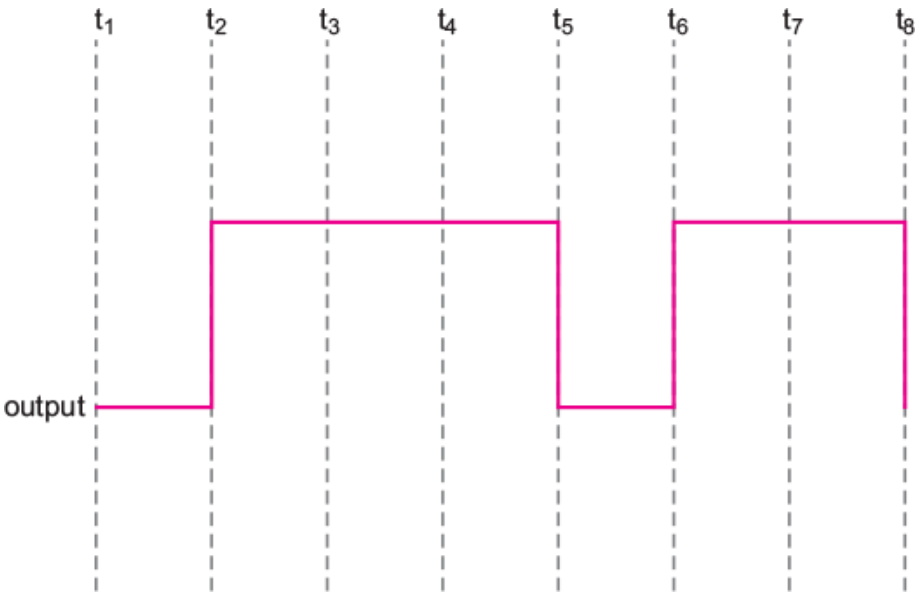
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

(ii) Output will be high if both inputs A and B are high., so B is in higher state in higher state in intervals from 3 to 5 and from 7 to 8.

Q. 11. The figure shows input waveforms A and B to a logic gate. Draw the output waveform for an OR gate. Write the truth table for this logic gate and draw its logic symbol. [CBSE (AI) 2017]



Ans.

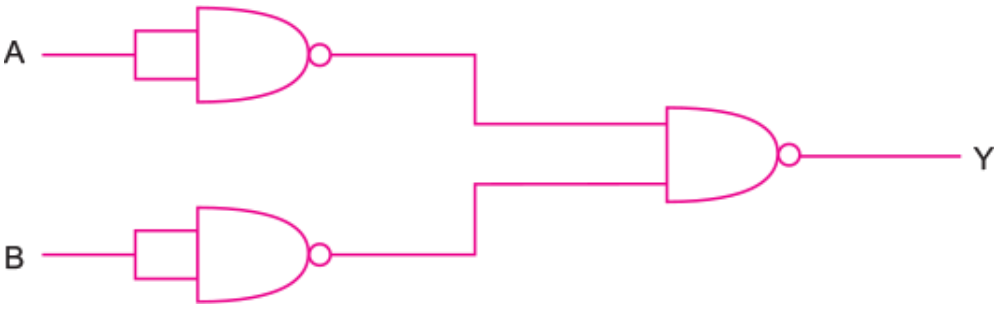


Truth Table

Input		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

OR Gate

Q. 12. Write the truth table for the logic circuit shown below and identify the logic operation performed by this circuit. [CBSE Delhi 2011, (AI) 2011, (F) 2014]



Ans.

The logic circuit performs OR-operation.

Truth table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

Q. 13. Using truth tables of AND gate and NOT gate, show that NAND gate is an AND gate followed by a NOT gate. Hence write the truth table of NAND gate.

Why are NAND gates called 'Universal Gates'? [CBSE Guwahati 2015]

Ans.

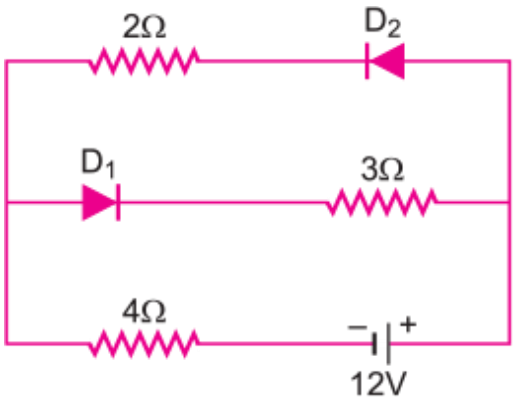
Input of AND Gate		Output of AND Gate and Input of NOT Gate	Output of NOT Gate
A	B		
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

Truth Table of NAND Gate

A	B	Output of NAND Gate
0	0	1
1	0	1
0	1	1
1	1	0

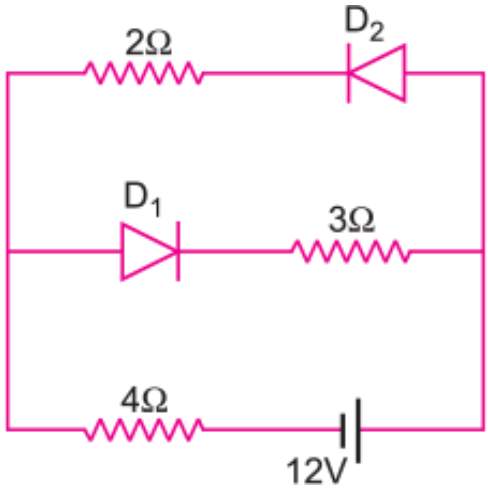
All primary gates like AND, NOT and OR gates can be realised by using NAND gate only. Hence, it is a universal gate.

Q. 14. The circuit shown in the figure has two oppositely connected ideal diodes connected in parallel. Find the current flowing through each diode in the circuit. [CBSE (F) 2013]



Ans. (i) Diode D_1 is reverse biased, so it offers an infinite resistance. So no current flows in the branch of diode D_1.

(ii) Diode D_2 is forward biased, and offers no resistance in the circuit. So current in the branch

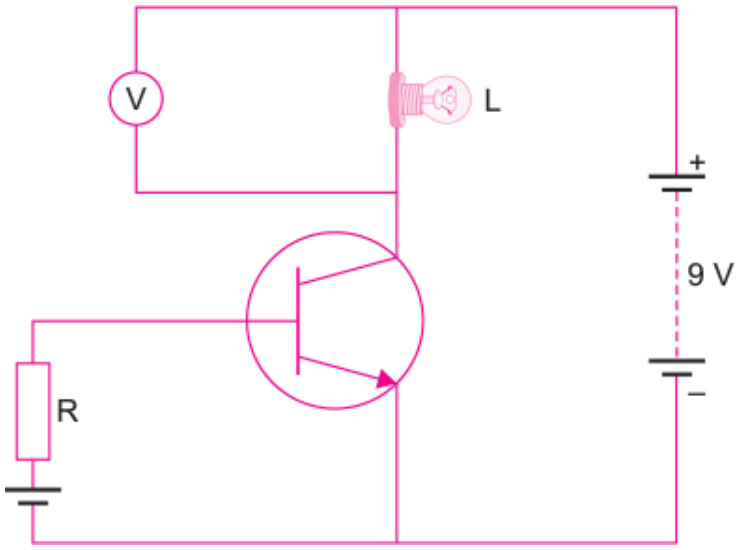


$$I = \frac{V}{R_{eq}} = \frac{12V}{2\Omega + 4\Omega} = 2A$$

Q 15. In the given circuit diagram, a voltmeter 'V' is connected across a lamp 'L'. How would (i) the brightness of the lamp and (ii) voltmeter reading 'V' be affected, if the value of resistance 'R' is decreased? Justify your answer.
[HOTS][CBSE Delhi 2013]

Ans. (i) If the value of the resistance *R* is reduced, the current in the forward biased input circuit increases. The emitter current IE and the collector current I_C (= I_E – I_B) both increase. Hence, the brightness of the lamp increases.

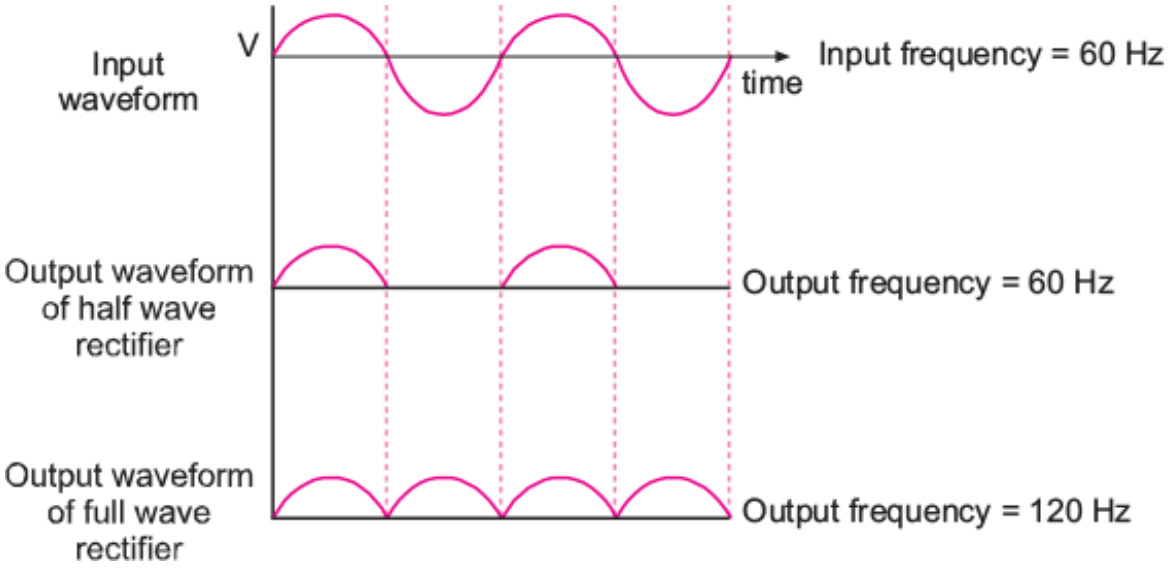
(ii) Due to increase in I_C, the potential drop across lamp *L* increases and hence the voltmeter reading *V* increases.



Short Answer Questions – I (OIQ)

Q. 1. An ac input signal of frequency 60 Hz is rectified by a (i) half wave (ii) full wave rectifier. Draw the output waveform and write the output frequency in each case.

Ans.



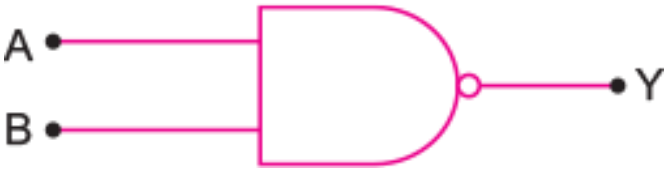
Q. 2. The following table gives the output of a two input logic gate.

(i) Identify the logic gate and draw its logic symbol.

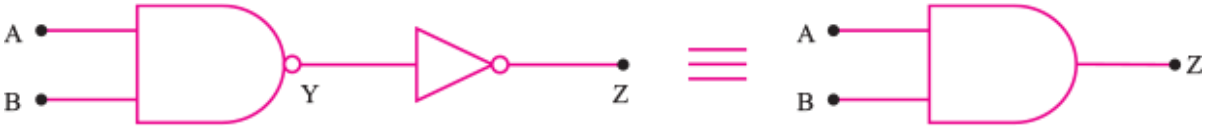
(ii) If the output of this gate is fed as input to a NOT gate, name the new logic gate so formed.

A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

Ans (i) The truth table given represents a NAND gate.



(ii) Clearly resulting gate will be an AND gate.

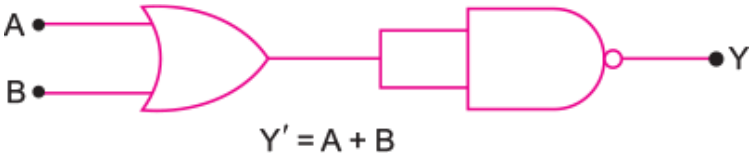


Truth table of new gate formed

Input		Output	
A	B	Y	$\bar{Y} = Z$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Q. 3. The output of an OR gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination of gates and write its truth table.

Ans. The logic circuit is shown in fig.



The logic circuit represents NOR gate. Its truth table is

A	B	Y'	Y
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

Q. 4. In a common emitter mode of a transistor, the d.c. current gain is 20, the emitter current is 7 mA. Calculate (i) base current and (ii) collector current.

Ans.

Given $\beta = 20$, $i_E = 7$ mA

i. $\beta = \frac{i_C}{i_B} = \frac{i_E - i_B}{i_B}$ or $\beta_{i\beta} = i_E - i_B$

$\Rightarrow \quad i_B = \frac{i_E}{\beta+1} = \frac{7 \text{ mA}}{20+1} = \frac{7}{21} \text{ mA} = \frac{1}{3} \text{ mA}$

ii. $i_C = i_E - i_B = 7 - \frac{1}{3} = \frac{20}{3}$ mA

Q. 5. A semiconductor has equal electron and hole concentration of 6 × 10^8 / m^3. On doping with certain impurity, electron concentration increases to 9 × 10^{12} / m^3.

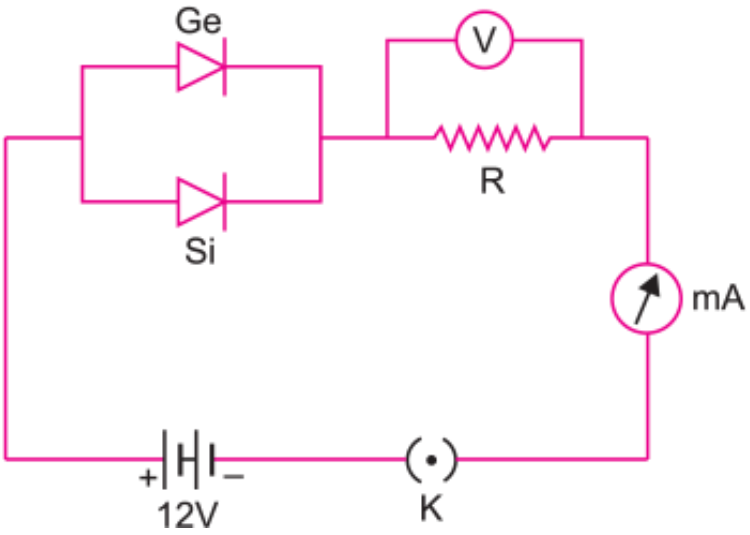
(i) Identify the new semiconductor obtained after doping.

(ii) Calculate the new hole concentration.

Ans. (i) The doped semiconductor is n-type.

ii. $n_e n_h = n_i^2 \quad \Rightarrow \quad n_h = \frac{n_i^2}{n_e} = \frac{(6\times10^8)^2}{9\times10^{12}} = 4 \times 10^4 \text{per m}^3$

Q. 6. Germanium and silicon junction diodes are connected in parallel. A resistance R, a 12 V battery, a milliammeter (mA) and key (K) are connected in series with them (figure). When key (K) is closed, a current begins to flow in the milliammeter. What will be the maximum reading of voltmeter connected across resistance R?
[HOTS]



Ans. The potential barrier of germanium junction diode is 0.3 V and of silicon is 0.7 V. Both germanium and silicon are forward biased. Therefore, for conduction the minimum potential difference across junction diode is 0.3 V.

Maximum reading of voltmeter connected across R = 12 – 0.3 = **11.7 V.**

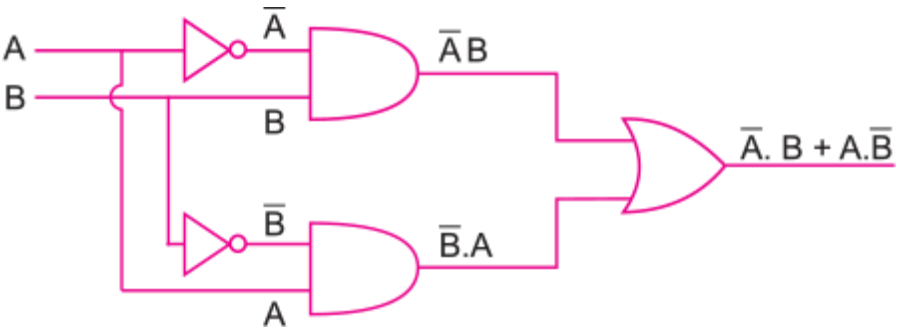
Q. 7. An X-OR gate has following truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

It is represented by following logic relation [HOTS][NCERT Exemplar]

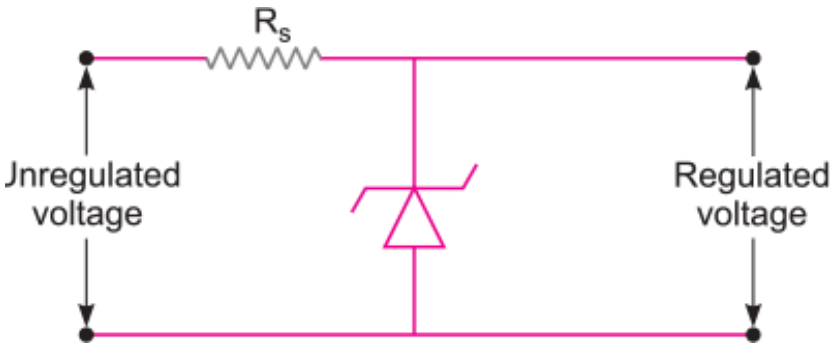
$Y = \bar{A}.\ B + A.\ \bar{B}$. Build this gate using AND, OR and NOT gates.

Ans.



Q. 8. A Zener of power rating 1 W is to be used as a voltage regulator. If zener has a breakdown of 5 V and it has to regulate voltage which fluctuated between 3 V

and 7 V, what should be the value of Rs for safe operation (see figure)? [HOTS][NCERT Exemplar]



Ans.

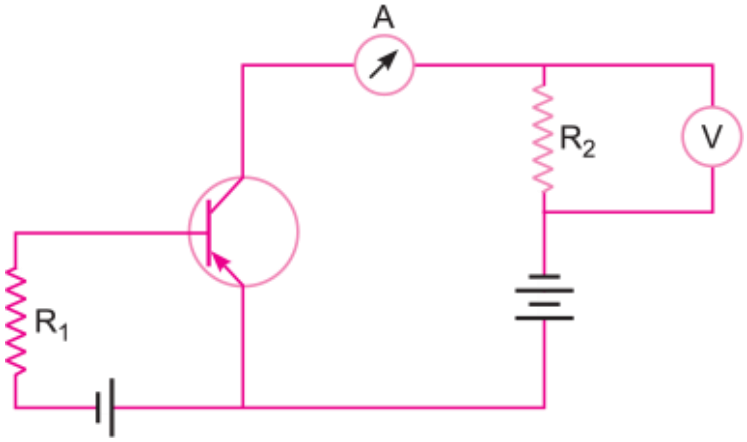
Here, P = 1W, V_z = 5V

V_s = 3V to 7V

$$I_{Z\ \max} = \frac{P}{V_Z} = \frac{1}{5} = 0.2A = 200\,\text{mA}$$

$$R_S = \frac{V_S - V_z}{I_{Z\ \max}} = \frac{7-5}{0.2} = \frac{2}{0.2} = 10\Omega$$

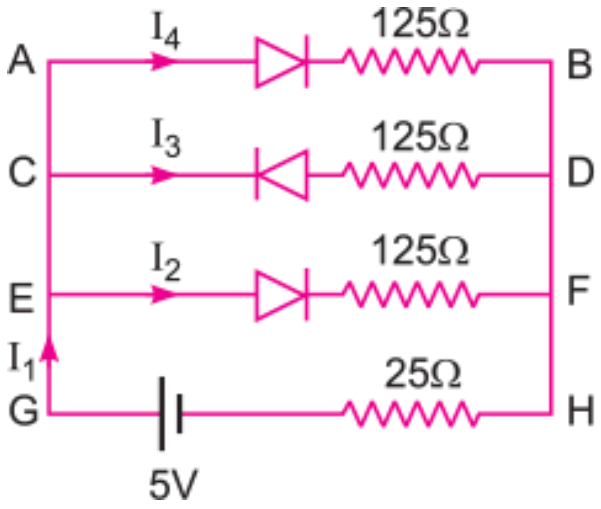
Q. 9. If the resistance R^1 is increased (Fig.), how will the readings of the ammeter and voltmeter change? [HOTS] [NCERT Exemplar]



Ans.

$I_B = \frac{V_{BB} - V_{BE}}{R_1}$. If R_1 is increased, I_B will decrease. Since $I_c = \beta I_b$, it will result in decrease in I_c, *i.e.*, decrease in ammeter and voltmeter readings.

Q. 10. If each diode in figure has a forward bias resistance of 25 Ω and infinite resistance in reverse bias, what will be the values of current I_1, I_2, I_3 and I_4? [HOTS] [NCERT Exemplar]



Ans. I_3 is zero as the diode in that branch is reverse biased. Resistance in the branch AB and EF are each (125 + 25)Ω = 150 Ω

As AB and EF are identical parallel branches, their effective resistance is $\frac{150}{2}$ = 75Ω

∴ Net resistance in the circuit = (75 + 25) Ω = 100 Ω

$$\therefore \text{Current } I_1 = \frac{5}{100} = 0.05A$$

As resistances of AB and EF are equal, and $I_1 = I_2 + I_3 + I_4$, $I_3 = 0$

$$\therefore I_2 = I_4 = \frac{0.05}{2} = 0.025\,A$$

Q. 11. Three photo diodes D_1, D_2 and D_3 are made of semiconductors having band gaps of 2.5 eV, 2 eV and 3 eV, respectively. Which ones will be able to detect light of wavelength 6000 Å? [HOTS][NCERT Exemplar]

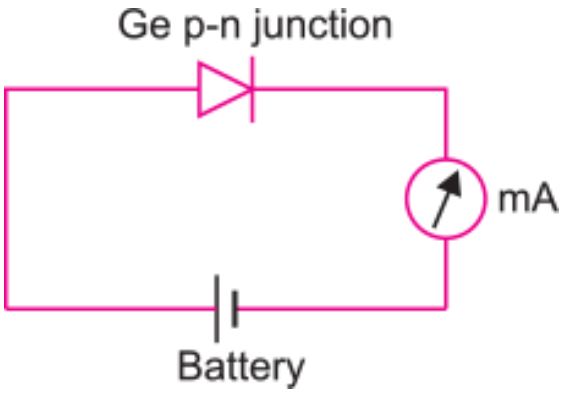
Ans. Energy of incident light photon,

$$E = h\nu = \frac{hc}{\lambda}$$

$$= \frac{6.6\times10^{-34}\times3\times10^{8}}{6\times10^{-7}\times1.6\times10^{-19}} = 2.06\ \text{eV}$$

For the incident radiation to be detected by the photodiode, energy of incident radiation photon should be greater than the band gap. This is true only for D_2. Therefore, only D_2 will detect this radiation.

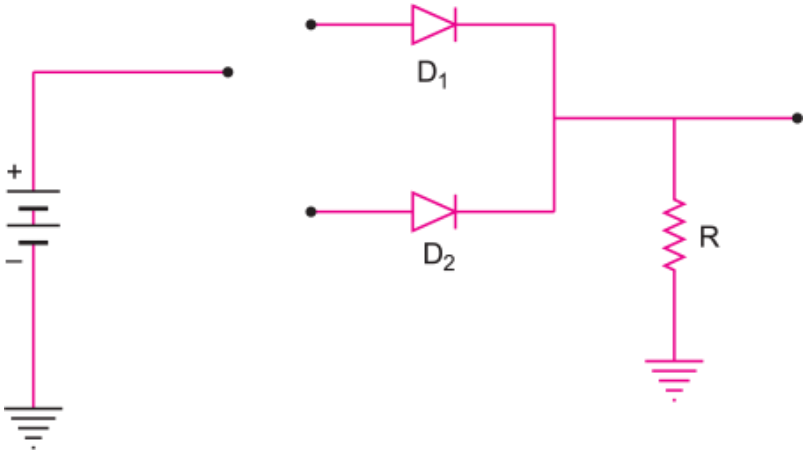
Q. 12. A germanium p-n junction is connected to a battery with milliammeter in series. What should be the minimum voltage of battery so that current may flow in the circuit?
[HOTS]



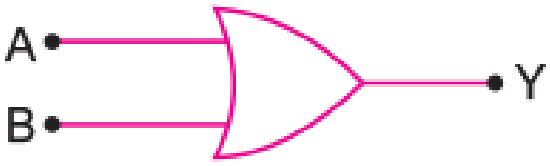
Ans. The internal potential barrier of germanium is 0.3 V, therefore to overcome this barrier the potential of battery should be equal to or more than 0.3 V.

Therefore, the minimum voltage of battery = 0.3 V.

Q. 13. Name the logic gate which can be realised by using a p-n junction diode in the given diagram. Give its logic symbol and write the truth table. Name the gate which will be obtained by combining with a NOT gate.



Ans. The logic gate shown in the circuit diagram is OR gate.



Symbol of OR gate:

Input		**Output**
A	**B**	**Y**
0	0	1
1	0	1
0	1	1
1	1	1

The gate obtained by combining OR gate with NOT gate will be NOR gate.

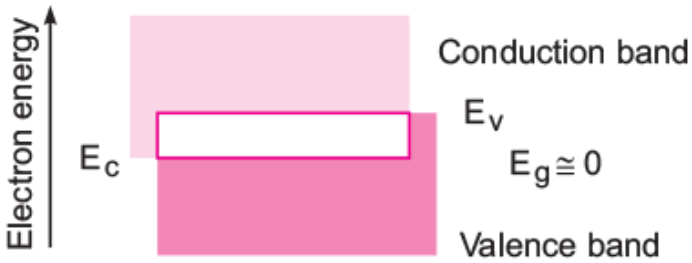
Short Answer Questions – II (PYQ)

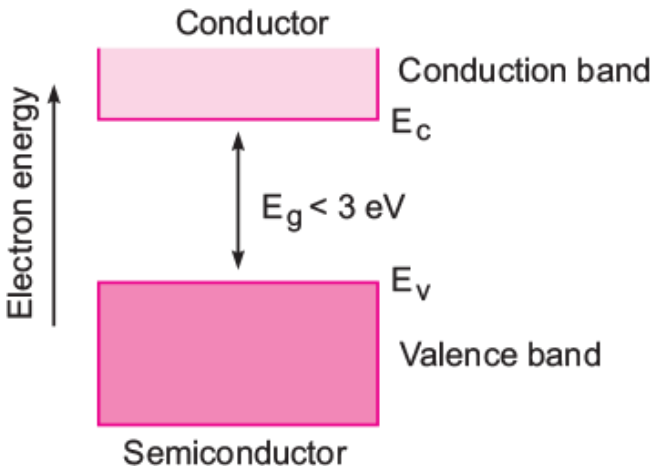
Q. 1. What are energy bands? Write any two distinguishing features between conductors, semiconductors and insulators on the basis of energy band diagrams.
[CBSE (AI) 2014, North 2016]

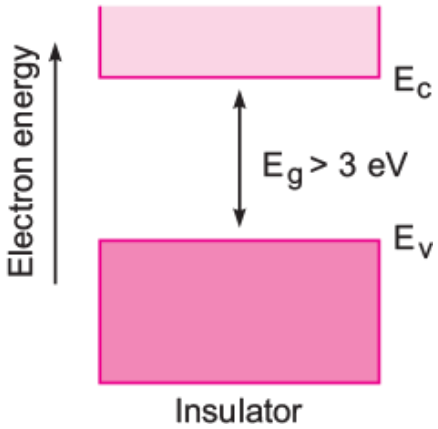
OR

Draw the necessary energy band diagrams to distinguish between conductors, semiconductors and insulators. How does the change in temperature affect the behaviour of these materials? Explain briefly. [CBSE Patna 2015]

Ans. Energy Bands: In a solid, the energy of electrons lie within certain range. The energy levels of allowed energy are in the form of bands, these bands are separated by regions of forbidden energy called band gaps.







Distinguishing features:

(a) In conductors: Valence band and conduction band overlap each other.

In semiconductors: Valence band and conduction band are separated by a small energy gap.

In insulators: They are separated by a large energy gap.

(b) In conductors: Large number of free electrons are available in conduction band.

In semiconductors: A very small number of electrons are available for electrical conduction.

In insulators: Conduction band is almost empty i.e., no electron is available for conduction.

Effect of Temperature:

(i) In conductors: At high temperature, the collision of electrons become more frequent with the atoms/molecules at lattice site in the metals as a result the conductivity decreases (or resistivity increases).

(ii) In semiconductors: As the temperature of the semiconducting material increases, more electron hole pairs becomes available in the conduction band and valance band, and hence the conductivity increases or the resistivity decreases.

(iii) In insulators: The energy band between conduction band and valance band is very large, so it is unsurpassable for small temperature rise. So, there is no change in their behaviour.

Q. 2. Distinguish between 'intrinsic' and 'extrinsic' semiconductors.
[CBSE Delhi 2015, (F) 2017]

Ans.

	Intrinsic semiconductor	**Extrinsic semiconductor**
(i)	It is a semiconductor in pure form.	It is a semiconductor doped with trivalent or pentavalent impurity atoms.
(ii)	Intrinsic charge carriers are electrons and holes with equal concentration.	The two concentrations are unequal in it. There is excess of electrons in n-type and excess of holes in p-type semiconductors.
(iii)	Current due to charge carriers is feeble (of the order of μ A).	Current due to charge carriers is significant (of the order of mA).

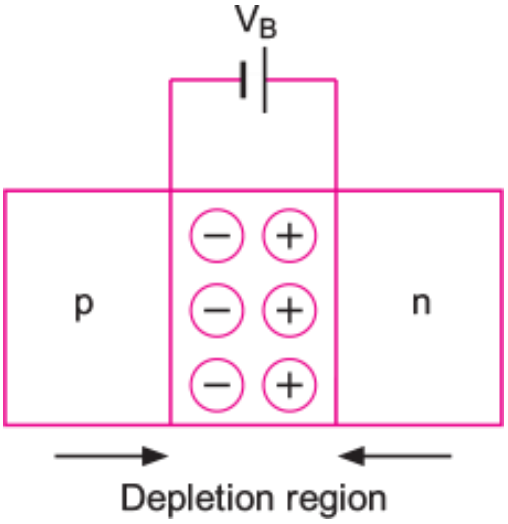
Q. 3. Distinguish between an intrinsic semiconductor and a p-type semiconductor. Give reason why a p-type semiconductor crystal is electrically neutral, although nh >> ne. [CBSE (F) 2013]

Ans.

	Intrinsic semiconductor	Extrinsic semiconductor
(i)	It is a semiconductor in pure form.	It is a semiconductor doped with p-type (like Al, In) impurity.
(ii)	Intrinsic charge carriers are electrons and holes with equal concentration.	Majority charge carriers are holes and minority charge carriers are electrons.
(iii)	Current due to charge carriers is feeble (of the order of μ A).	Current due to charge carriers is significant (of the order of mA).

p-type semiconductor is electrically neutral because every atom, whether it is of pure semiconductor (Ge or Si) or of impurity (Al) is electrically neutral.

Q. 4. Name the important process that occurs during the formation of a p-n junction. Explain briefly, with the help of a suitable diagram, how a p-n junction is formed. Define the term 'barrier potential'. [CBSE (F) 2011, Central 2016]



Ans. Potential barrier: During the formation of a p-n junction the electrons diffuse from n-region to p-region and holes diffuse from p-region to n-region. This forms recombination of charge carriers. In this process immobile positive ions are collected at a junction toward n-region and negative ions at a junction toward p-region. This causes a potential difference across the unbiased junction. This is called potential barrier.

Depletion region: It is a layer formed near the junction which is devoid of free charge carriers. Its thickness is about 1 μm.

Q. 5. Explain, with the help of a circuit diagram, the working of a photo-diode. Write briefly how it is used to detect the optical signals. [CBSE Delhi 2013]

OR

(a) How is photodiode fabricated?

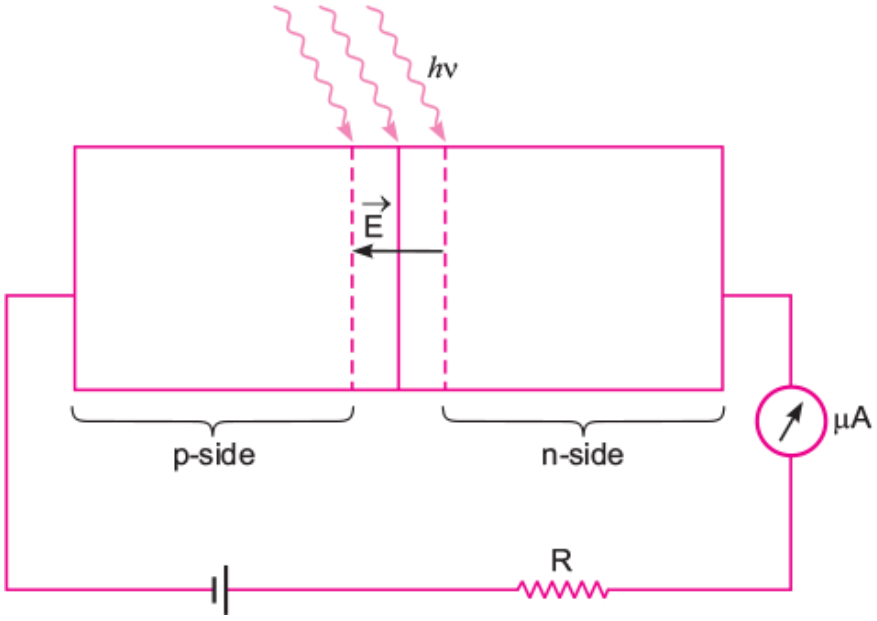
(b) Briefly explain its working. Draw its V–I characteristics for two different intensities of illumination. [CBSE (F) 2014]

OR

With what considerations in view, a photodiode is fabricated? State its working with the help of a suitable diagram.

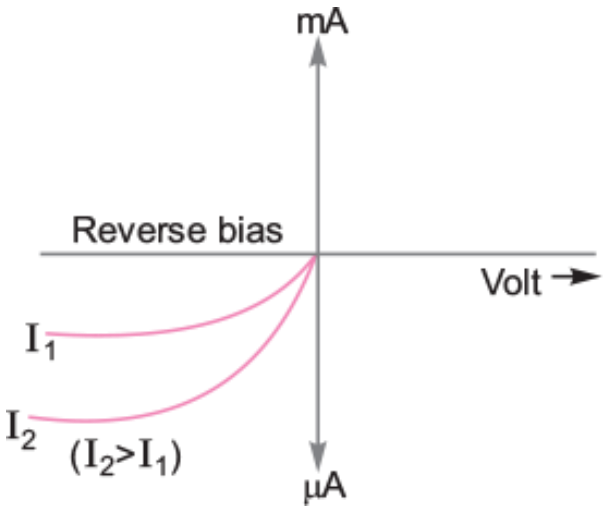
Even though the current in the forward bias is known to be more than in the reverse bias, yet the photodiode works in reverse bias. What is the reason? [CBSE Delhi 2015, East 2016]

Ans. A photo-diode is fabricated using photosensitive Semiconducting material with a transparent window to allow light to fall on the junction of the diode.



Working: In diode (any type of diode), an electric field 'E' exists across the junction from *n*-side to *p*-side, when light with energy hv greater than energy gap E_g ($h_v > E_g$) illuminates the junction, then electron- hole pairs are generated due to absorption of photons, in or near the depletion region of the diode. Due to existing electric field, electrons and holes get separated. The free electrons are collected on *n*-side and holes are collected on *p*-side, giving rise to an emf.

Due to the generated emf, an electric current of μ*A* order flows through the external resistance.



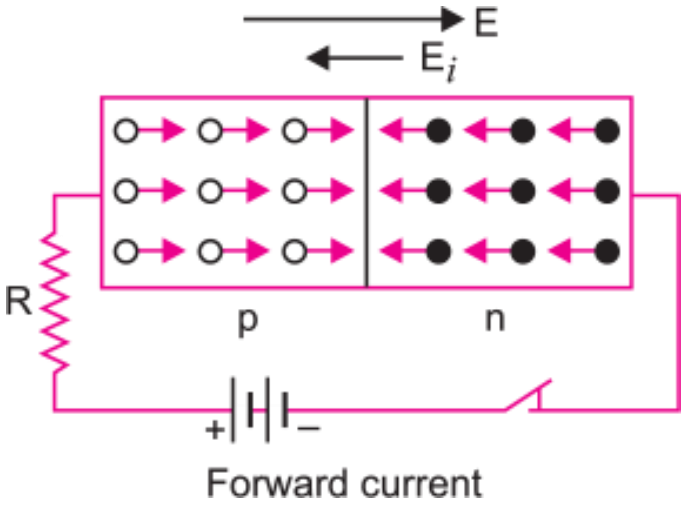
Detection of Optical Signals:

It is easier to observe the change in the current with change in the light intensity if a reverse bias is applied. Thus, photodiode can be used as a photodetector to detect optical signals.

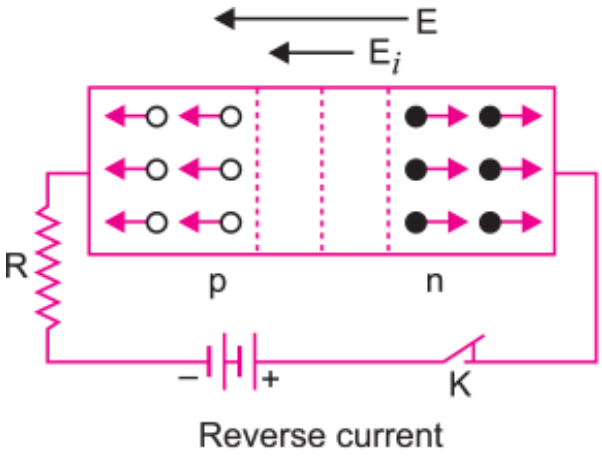
The characteristic curves of a photodiode for two different illuminations I_1 and I_2 ($I_2 > I_1$) are shown.

Q. 6. Explain how the width of depletion layer in a p-n junction diode changes when the junction is (i) forward biased (ii) reverse biased. [CBSE (AI) 2009]

Ans. (i) Under forward biasing the applied potential difference causes a field which acts opposite to the potential barrier. This results in reducing the potential barrier, and hence the width of depletion layer decreases.



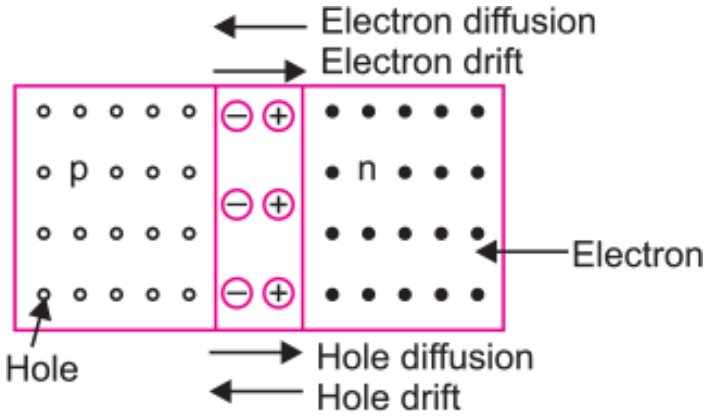
(ii) Under reverse biasing the applied potential difference causes a field which is in the same direction as the field due to internal potential barrier. This results in an increase in barrier voltage and hence the width of depletion layer increases.



Q. 7. Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a p-n junction. [CBSE (AI) 2012, Bhubaneshwar 2015]

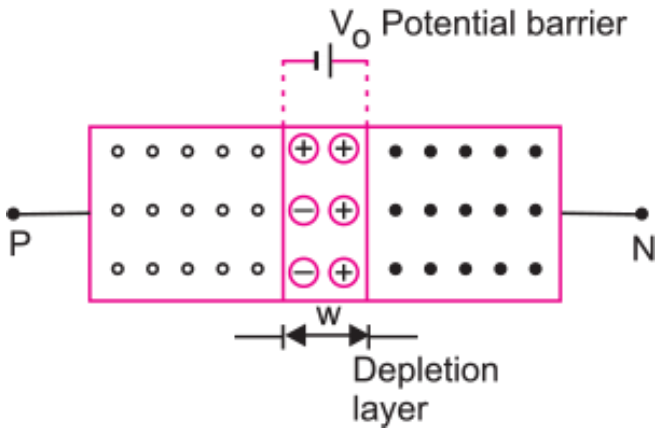
Ans. Two important processes occurring during the formation of a p-n junction are (i) diffusion and (ii) drift.

(i) Diffusion: In n-type semiconductor, the concentration of electrons is much greater as compared to concentration of holes; while in p-type semiconductor, the concentration of holes is much greater than the concentration of electrons. When a p-n junction is formed, then due to concentration gradient, the holes diffuse from p-side to n-side (p → n) and electrons diffuse from n-side to p-side (n → p). This motion of charge carriers gives rise to diffusion current across the junction.



(ii) Drift: The drift of charge carriers occurs due to electric field. Due to built in potential barrier, an electric field directed from n-region to p-region is developed across the junction. This field causes motion of electrons on p-side of the junction to n-side and

motion of holes on n-side of junction to p-side. Thus a drift current starts. This current is opposite to the direction of diffusion current.



Q. 8. How is a light emitting diode fabricated? Briefly state its working. Write any two important advantages of LEDs over the conventional incandescent low power lamps.
[CBSE Bhubaneshwar 2015]

OR

(a) Explain briefly the process of emission of light by a Light Emitting Diode (LED).

(b) Which semiconductors are preferred to make LEDs and why?

(c) Give two advantages of using LEDs over conventional incandescent lamps.
[CBSE South 2016]

Ans. LED is fabricated by

(i) Heavy doping of both the *p* and *n* regions.

(ii) Providing a transparent cover so that light can come out.

Working: When the diode is forward biased, electrons are sent from $n \rightarrow p$ and holes from $p \rightarrow n$. At the junction boundary, the excess minority carriers on either side of junction recombine with majority carriers. This releases energy in the form of photon $h_v = E_g$.

GaAs (Gallium Arsenide): Band gap of semiconductors used to manufacture LED's should be 1.8 eV to 3eV. These materials have band gap which is suitable to produce desired visible light wavelengths.

Advantages

(i) Low operational voltage and less power consumption.

(ii) Fast action and no warm-up time required.

(iii) Long life and ruggedness.

(iv) Fast on-off switching capability.

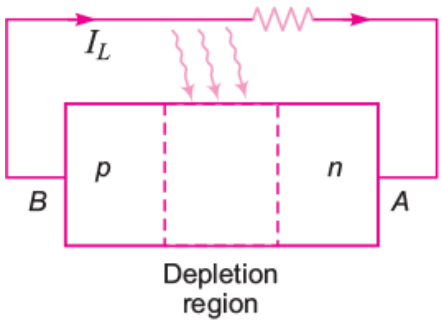
Q. 9. Describe briefly using the necessary circuit diagram, the three basic processes which take place to generate the emf in a solar cell when light falls on it. Draw the I – V characteristics of a solar cell. Write two important criteria required for the selection of a material for solar cell fabrication. [CBSE Guwahati 2015]

OR

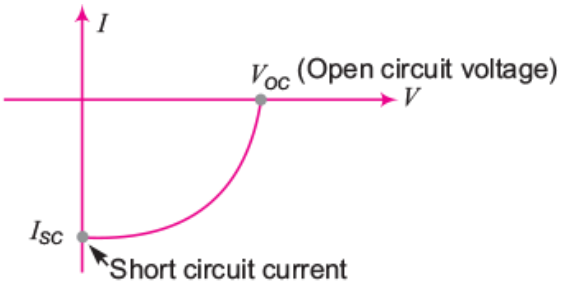
(i) Describe the working principle of a solar cell. Mention three basic processes involved in the generation of emf.

(ii) Why are Si and GaAs preferred materials for solar cells? [CBSE (F) 2016]

Ans. Principle: It is based on photovoltaic effect (generation of voltage due to bombardment of light photons). When solar cell is illuminated with light photons of energy (hv) greater than the energy gap (E_g) of the semiconductor, then electron-hole pairs are generated due to absorption of photons.



(a)



(b)

The three basic processes involved are: generation, separation and collection

a. generation of electron-hole pairs due to light (with $h_v > E_g$) close to the junction
b. Separation of electrons and holes due to electric field of the depletion region. Electrons are swept to *n*-side and holes to *p*-side
c. the electrons reaching the *n*-side are collected by the front contact and holes reaching *p*-side are collected by the back contact. Thus, *p*-side becomes positive and *n*-side becomes negative giving rise to photo voltage.

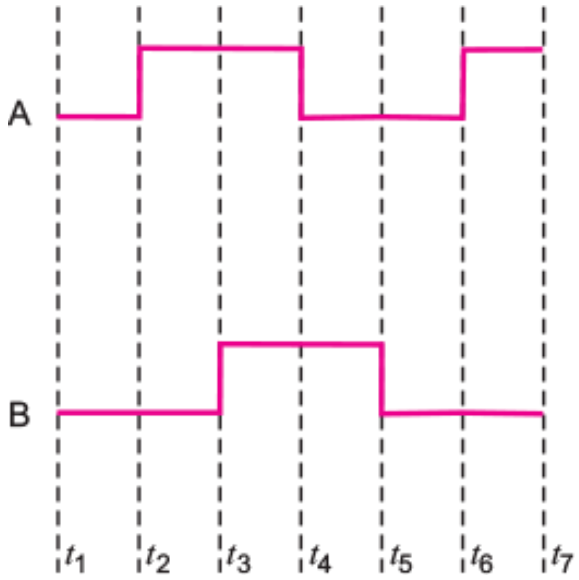
Important criteria for the selection of a material for solar cell fabrication are:

i. band gap (~1.0 to 1.8 eV),
ii. high optical absorption (–10^4 cm^{-1}),
iii. electrical conductivity,
iv. availability of the raw material, and
v. cost

Solar radiation has maximum intensity of photons of energy = 1.5 eV

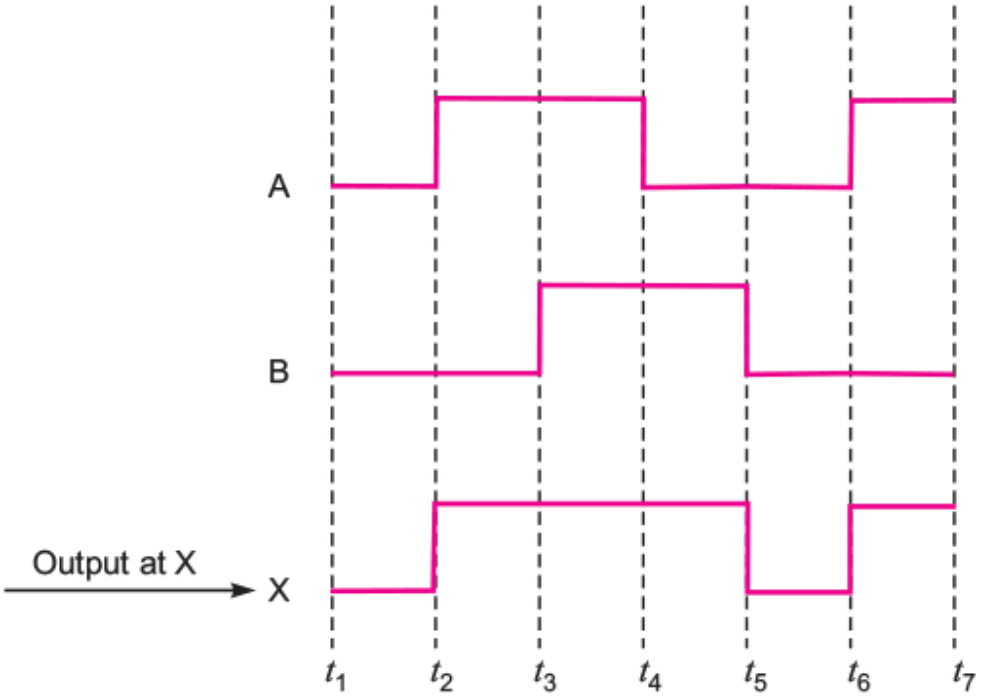
Hence semiconducting materials Si and GaAs, with band gap ≈ 1.5 eV, are preferred materials for solar cells.

Q. 10. Draw the output waveform at X, using the given inputs A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit. [CBSE Delhi 2011]

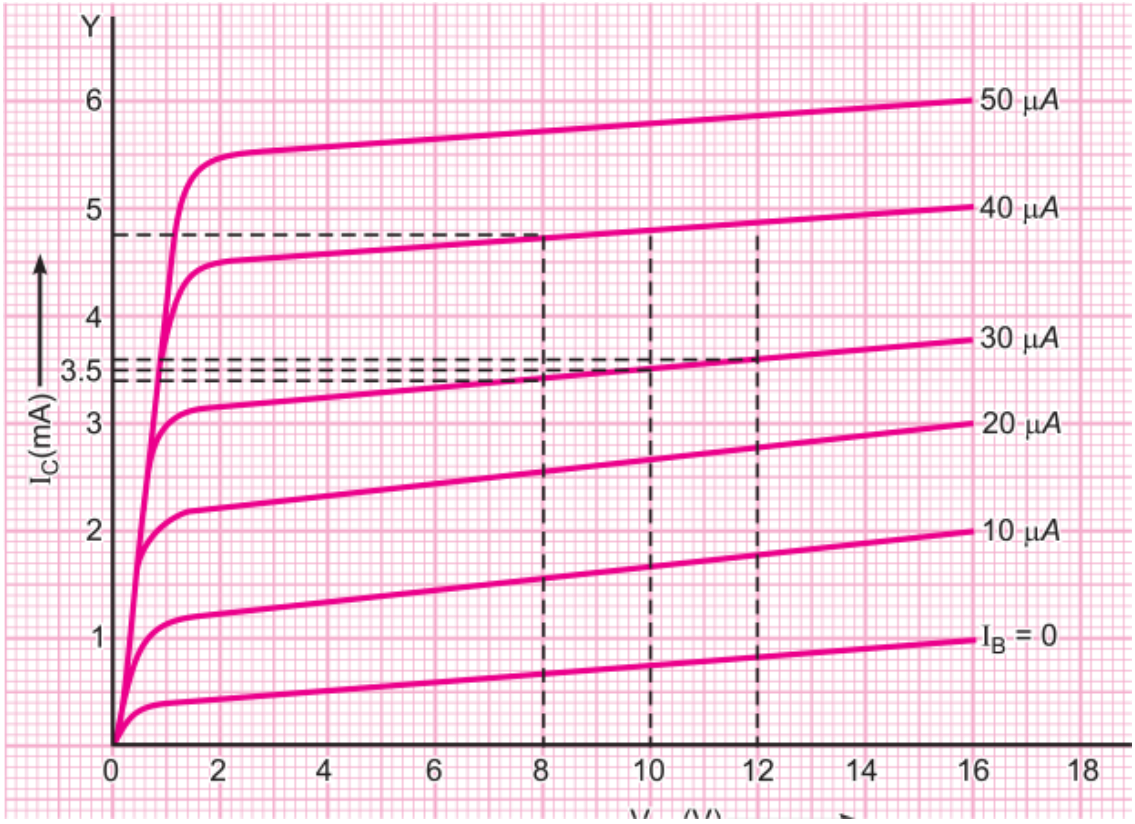


Ans. $X = \bar{Y} = A + B$

The given circuit performs OR operation



Q. 11. Output characteristics of an n-p-n transistor in CE configuration is shown in the figure. Determine: [CBSE Delhi 2013]



(i) Dynamic output resistance
(ii) Dc current gain and
(iii) ac current gain at an operating point V_{CE} = 10 V, when I_B = 30 μA.

Ans. (i) Dynamic output resistance is given by

$$r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$$

For $I_B = 30\ \mu A$, $\Delta V_{CE} = (12 - 8) = 4V$ and $\Delta I_C = (3.6 - 3.4) = 0.2\ mA$

$$\therefore \quad r_o = \frac{4V}{0.2\ mA} = \frac{4}{0.2\times10^{-3}} = 2 \times 10^4\ \text{ohm}$$

(ii)

$$\beta_{dc} = \frac{I_C}{I_B}$$

At $V_{CE} = 10$ V and $I_B = 30\ \mu$ A, the value of $I_C = 3.5$m A

$$\beta_{dc} = \frac{3.5\ mA}{30\ \mu A} = \frac{3.5\times10^{-3}}{30\times10^{-6}} \quad \Rightarrow \quad \beta_{dc} = 117$$

(iii)

$$\text{ac current gain } \beta_{dc} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

At V_{CE} =10 V, $\Delta I_C = (3.5 - 2.5)\ mA = 1\ mA$

and $\Delta I_B = (30\ \mu A - 20\ \mu A) = 10\ \mu A$

$$\therefore \quad \beta_{dc} = \frac{1\ mA}{10\mu A} = 100$$

Q. 12. Draw V – I characteristics of a p–n junction diode. Answer the following questions, giving reasons:

(i) Why is the current under reverse bias almost independent of the applied potential upto a critical voltage?

(ii) Why does the reverse current show a sudden increase at the critical voltage?

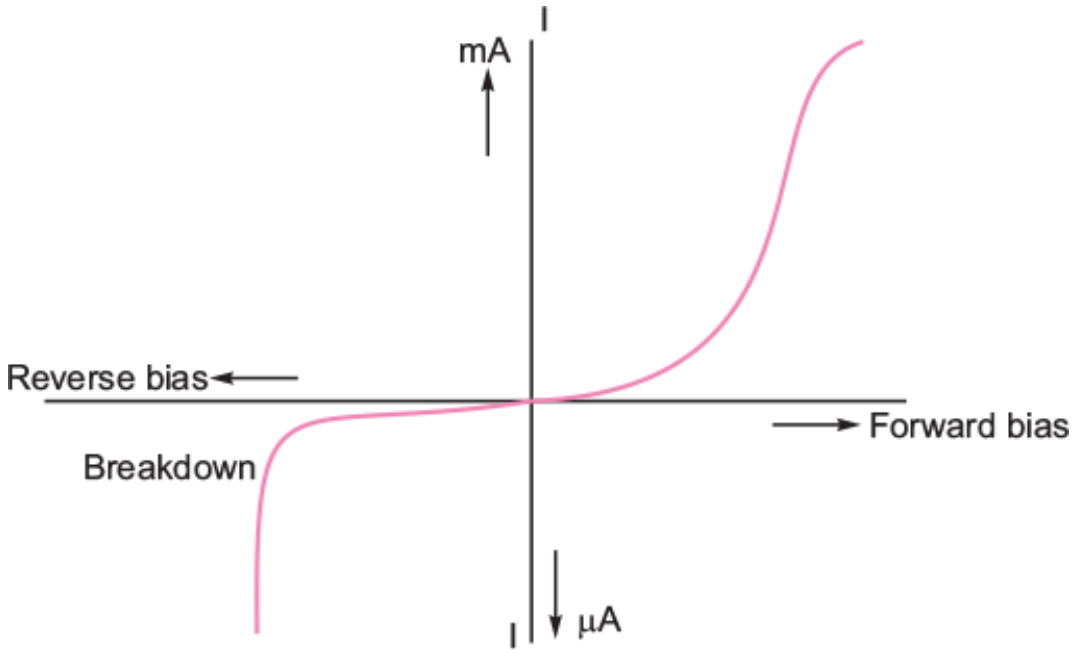
Name any semiconductor device which operates under the reverse bias in the breakdown region. [CBSE (AI) 2013]

Ans. (i) In the reverse biasing, the current of order of μA is due to movement/drifting of minority charge carriers from one region to another through the junction.

A small applied voltage is sufficient to sweep the minority charge carriers through the junction. So, reverse current is almost independent of critical voltage.

(ii) At critical voltage (or breakdown voltage), a large number of covalent bonds break, resulting in the increase of large number of charge carriers. Hence, current increases at critical voltage.

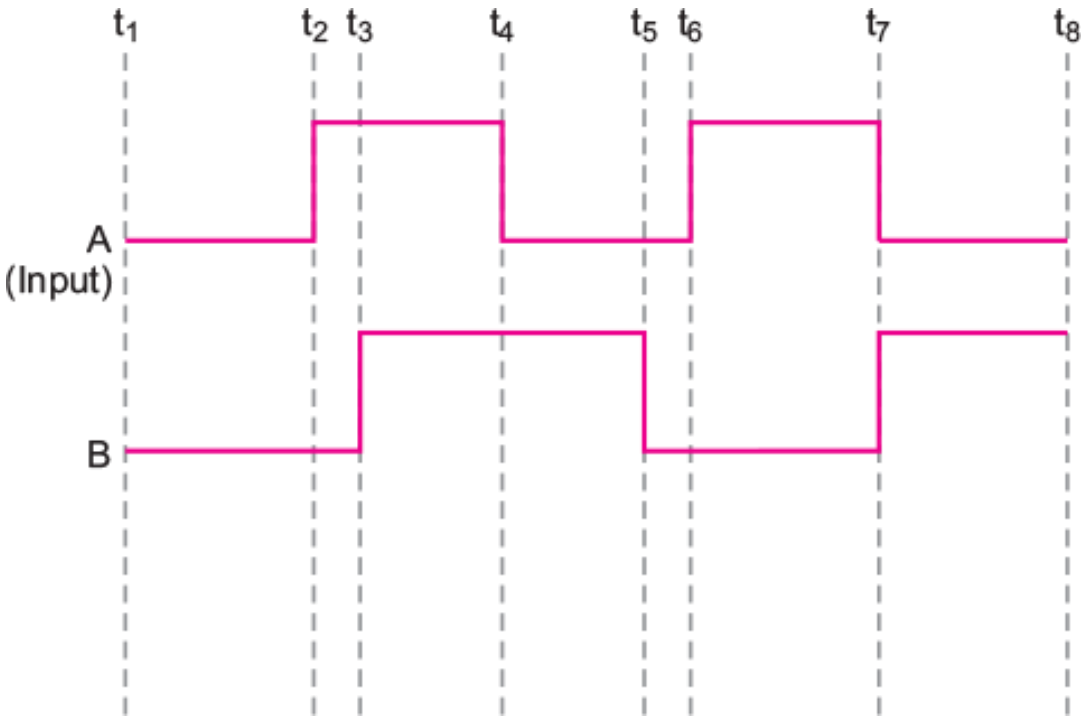
Semiconductor device that is used in reverse biasing is zener diode.



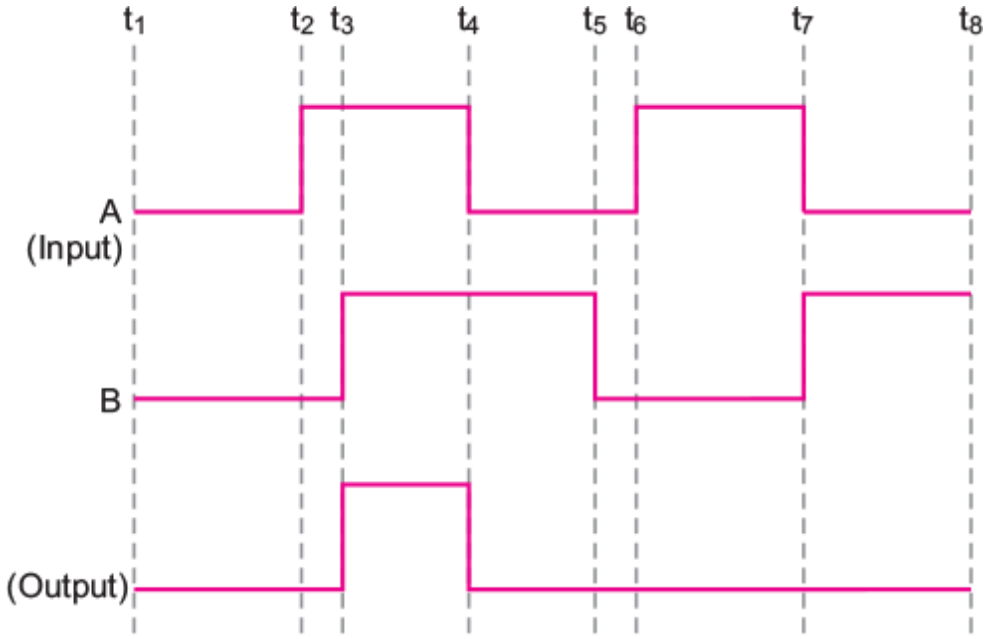
Q. 13. Answer the following question:

(i) Write the functions of the three segments of a transistor.

(ii) The figure shows the input waveforms A and B for 'AND' gate. Draw the output waveform and write the truth table for this logic gate. CBSE (AI) 2017]



Ans. Output waveform for AND gate is



Truth Table

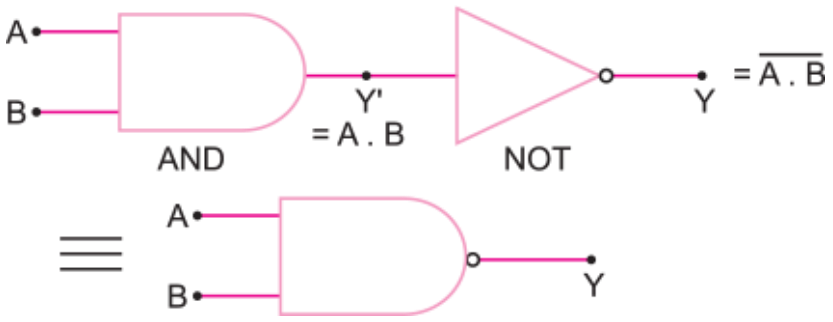
Input		Output
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

Q. 14. The following figure shows the input waveforms (A, B) and the output waveform (Y) of a gate. Identify the gate, write its truth table and draw its logic symbol.
[CBSE North 2016]

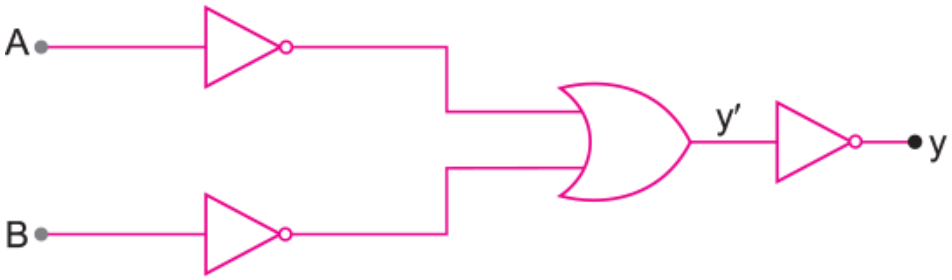
Ans. Gate is **NAND** Gate.

Truth Table

Input		Output
A	B	$Y = \overline{A.B}$
0	0	1
1	0	1
0	1	1
1	1	0



Q. 15. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table. [CBSE (AI) 2013]



Ans. AND Gate

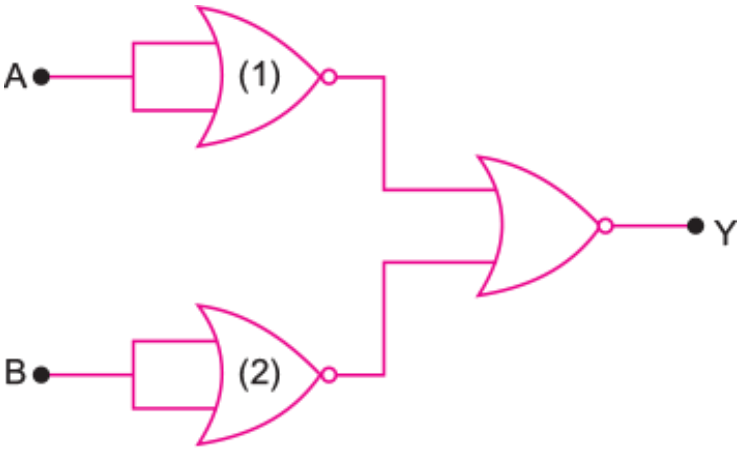
Truth Table

A	B	$Y = \bar{A}.\bar{B}$
0	0	0
1	0	0
0	1	0
1	1	1

Extended Truth Table

A	B	$\bar{A}$	$\bar{B}$	$Y' = \bar{A} + \bar{B}$	$y = \bar{\bar{A} + \bar{B}}$
0	0	1	1	1	0
1	0	0	1	1	0
0	1	1	0	1	0
1	1	0	0	0	1

Q. 16. The inputs A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown below. [CBSE (AI) 2011, (F) 2014]



Analyse the action of the gates (1) and (2) and identify the logic gate of the complete circuit so obtained. Give its symbol and truth table.

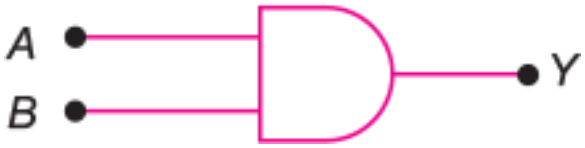
Ans.

Output of gate (1), $Y_1 = A \bar{+} A = \bar{A}$

Output of gate (2), $Y_2 = B \bar{+} B = \bar{B}$

Output $Y = Y_1 \bar{+} Y_2 = \bar{A} \bar{+} \bar{B} = \bar{\bar{A}} \,.\, \bar{\bar{B}} = \mathrm{AB}$

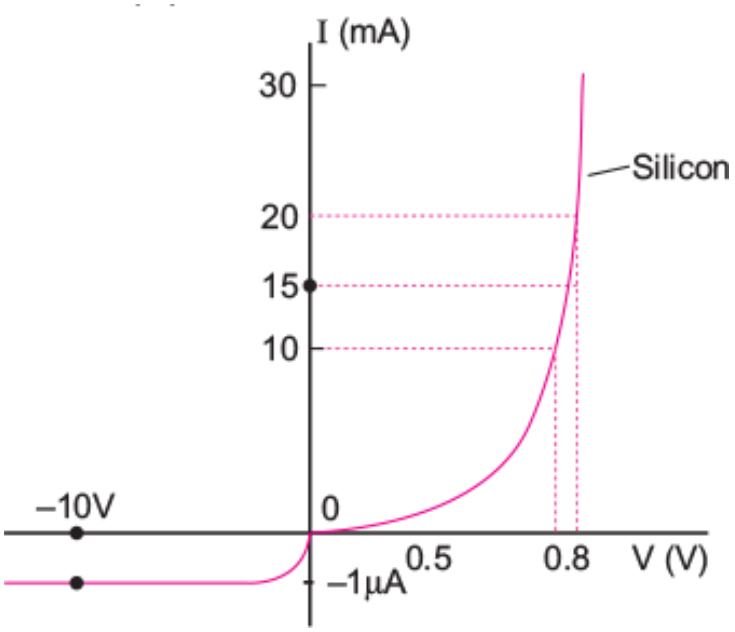
Thus, gates (1) and (2) act on '**NOT**' gates and the complete circuit acts as '**AND**' gate. The symbol and truth table of complete circuit are given below:



Truth Table

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

Q. 17. The V – I characteristic of a silicon diode is as shown in the figure. Calculate the resistance of the diode at (i) I = 15 mA and (ii) V = – 10 V. [CBSE (F) 2015]



Ans. (i) By considering straight line of *V–I* characteristic curve between 10 mA to 20 mA; and assuming passing through the origin, draw horizontal and vertical lines from 10 mA and 20 mA, we have

I_1 = 10 mA, V_1 = 0.7 V

and I_2 = 20 mA, V_2 = 0.8 V

Dynamic resistance in forward biasing can be given as

$$R = \frac{\Delta V}{\Delta I} = \frac{(0.8 - 0.7)V}{(20 - 10)\ \text{mA}}$$

$$= \frac{0.1V}{10\ \text{mA}} = \frac{0.1}{10} \times 10^3\ \Omega = 10\ \Omega$$

(ii) At – 10 V. The *V–I* characteristic graph is a straight line parallel to the voltage axis and not showing any variation. So, the static resistance can be given as

V = – 10 V and I = –1 μA

$$\therefore \text{Static resistance, } R = \frac{V}{I} = \frac{10\ V}{1\mu A} = \frac{10}{1\times10^{-6}} = 10^7\Omega$$

Q. 18. The current in the forward bias is known to be more (~mA) than the current in the reverse bias (~μA). What is the reason, then, to operate the photodiode in reverse bias? [HOTS][CBSE Delhi 2012]

Ans. Consider the case of n-type semiconductor. The majority carrier (electron) density is larger than the minority hole density, i.e., n >> p.

On illumination, the no. of both types of carriers would equally increase in number as

n' = n + Δn, p' = p + Δp

But Δn = Δp and n >> p

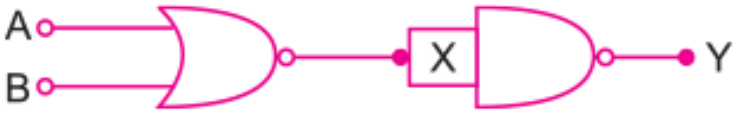
Hence, the fractional change in majority carrier, i.e, $\frac{\Delta n}{n} << \frac{\Delta p}{p}$ (fractional change in minority carrier)

Fractional change due to photo-effects on minority carrier dominated reverse bias current is more easily measurable than the fractional change in majority carrier dominated forward bias current. Hence photodiodes are used in reverse bias condition for measuring light intensity.

Q. 19. Answer the following question : [CBSE (F) 2015]

(i) What is an 'integrated circuit (I.C.)'? Distinguish between (i) linear I.C. and (ii) Digital I.C.

(ii) Identify the equivalent gate for the following circuit and write its truth table.



The output of NOR gate is connected to both the inputs of NAND gate.

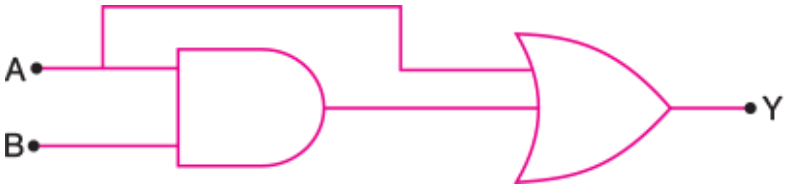
The equivalent gate is OR gate.

Input		Output	
A	B	X	Y
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Short Answer Questions – II (OIQ)

Q. 1. Answer the following question :

(i) Write the truth table of the following gate.



(ii) What will be the values of inputs A and B for the Boolean expression
$(A \bar{+} B).(A \bar{.} B) = 1$

Ans. (i) Truth table of the given gate

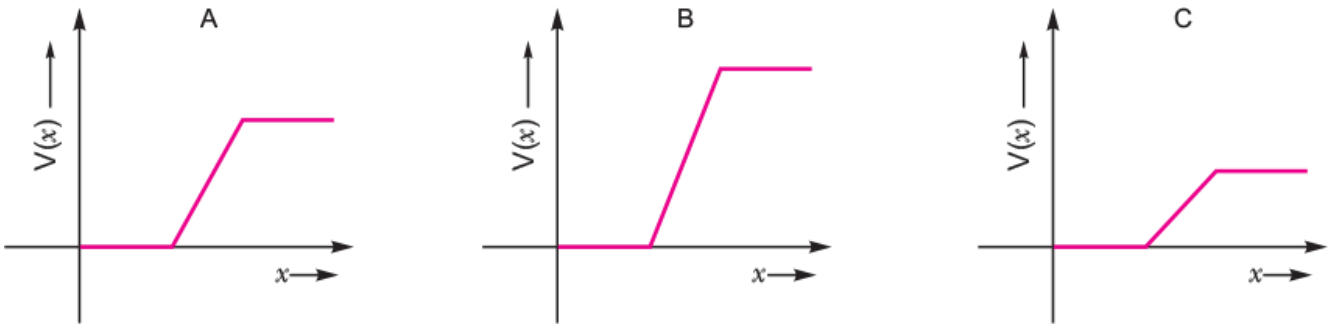
Input		Output
A	B	$Y = A + AB$
0	0	0
1	0	1
0	1	0
1	1	1

(ii)

$A = 0, B = 0$

Other then $(A \bar{+} B).(\bar{A}\bar{B}) = (0 \bar{+} 0)(0 \bar{.} 0) = \bar{0} \,.\, \bar{0} = 1 \,.\, 1 = 1$

Q. 2. The graph of potential barrier versus width of depletion region for an unbiased diode is shown in A. In comparison to A, graphs B and C are obtained after biasing the diode in different ways. Identify the type of biasing in B & C and justify your answer.
[CBSE Sample Paper 2016]



Ans. B : Reverse biased

Justification: When an external voltage *V* is applied across the semiconductor diode such that *n*-side is positive and *p*-side is negative, the direction of applied voltage is same as the direction of barrier potential. As a result, the barrier height increases and the depletion region widens due to the change in the electric field. The effective barrier height under reverse bias is ($V_0 + V$).

C : Forward biased

Justification: When an external voltage *V* is applied across a diode such that *p*-side is positive and *n*-side is negative, the direction of applied voltage (*V*) is opposite to the barrier potential (V_0). As a result, the depletion layer width decreases and the barrier height is reduced. The effective barrier height under forward bias is ($V_0 - V$).

Q. 3. A semiconductor has equal electron and hole concentration of 2×10^8 / m^3. On doping with a certain impurity, the hole concentration increases to 4×10^{10} / m^3.

(i) What type of semiconductor is obtained on doping?
(ii) Calculate the new electron and hole concentration of the semiconductor.
(iii) How does the energy gap vary with doping?

Ans. (i) Given $n_e = 2 \times 10^8$ / m^3, $n_h = 4 \times 10^{10}$ / m^3

(i) The majority charge carriers in doped semiconductor are holes, so semiconductor obtained is *p*-type semiconductor.

ii. $n_e n_h = n_i^2 \Rightarrow n_h = \frac{n_i^2}{n_h} = \frac{(2\times10^8)^2}{4\times10^{10}} = 10^6/m^3$

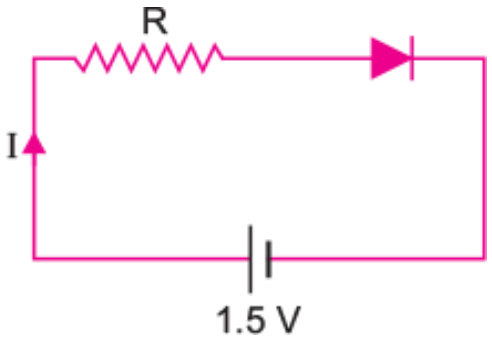
New electron concentration = 10^6 / m^3

hole concentration = 4×10^{10} / m^3

iii. Energy gap decreases on doping.

Q. 4. A p-n junction germanium diode when forward biased has a drop of 0.3 V which is assumed to be independent of current. The current in excess of 10 mA

through the diode produces a large Joule-heating which damages (burns) the diode. If we want to use a 1.5 V battery to forward-bias the diode, what should be the value of resistor used in series with the diode, so that the maximum current does not exceed 6 mA?

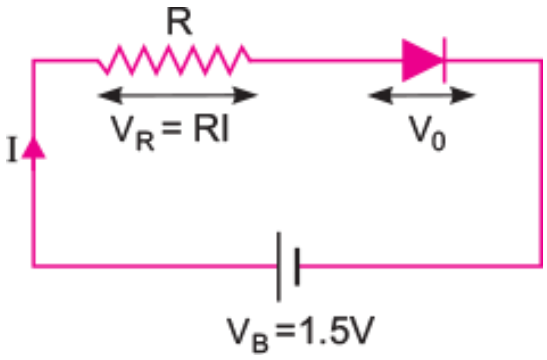


Ans. The basic equation of diode-circuit is

$$RI + V_0 = V_B \quad \Rightarrow \quad R = \frac{V_B - V_0}{I}$$

Here , V_B = 1.5 V, V_0 = 0.3 V, I = 5 mA = 6×10^{-3} A

$$\therefore \quad R = \frac{1.5 - 0.3}{6 \times 10^{-3}} = \frac{1.2 \times 10^3}{6} = 0.2 \times 10^3\ \Omega = 200\ \Omega$$



Q. 5. A change of 0.2 mA in the base current causes a change of 5 mA in the collector current for a common emitter amplifier.

(i) Find the ac current gain of the transistor.

(ii) If the input resistance is 2 kΩ and its voltage gain is 75, calculate the load resistor used in the circuit.

Ans. (i)

$$\text{ac current gain, } \beta = \frac{\Delta I_C}{\Delta I_B} = \frac{5 \text{ mA}}{0.2 \text{ mA}} = 25$$

(ii)

$$\text{Voltage gain, } A_v = \beta \frac{R_L}{R_i}$$

$$\text{Load resistance } R_L = \frac{A_v R_i}{\beta} = \frac{75 \times 2 \times 10^3}{25} = 60 \times 10^3\,\Omega = 6\,k\Omega$$

Q. 6. In a silicon transistor, the base current is changed by 20 μA. This results in a change of 0.02 V in base to emitter voltage and a change of 2 mA in the collector current.

(a) Find the input resistance, β_{ac} and trans conductance of the transistor.

(b) This transistor is used as an amplifier in CE configuration with a load resistance 5 kΩ. What is the voltage gain of the amplifier?

Ans. Given ΔI_B = 20 μA = 20 × 10^{-3} mA = 0.020 mA,

ΔV_{BE} = 0.02 V, ΔI_C = 2 mA

$$\text{a. Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.02}{20 \times 10^{-6}}\,\Omega = 10^3\,\Omega = 1k\Omega$$

$$\text{Current gain, } \beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{2 \text{ mA}}{0.020 \text{ mA}} = 100$$

Trans conductance of a transistor is defined as the ratio of change in collector current to the change in base to emitter voltage at constant collector to emitter voltage, i.e.,

$$g_m = \left(\frac{\Delta I_C}{\Delta V_{BE}}\right)_{V_{CE}=\text{constant}} = \frac{2 \times 10^{-3}}{0.02} = 0.1 W^{-1}$$

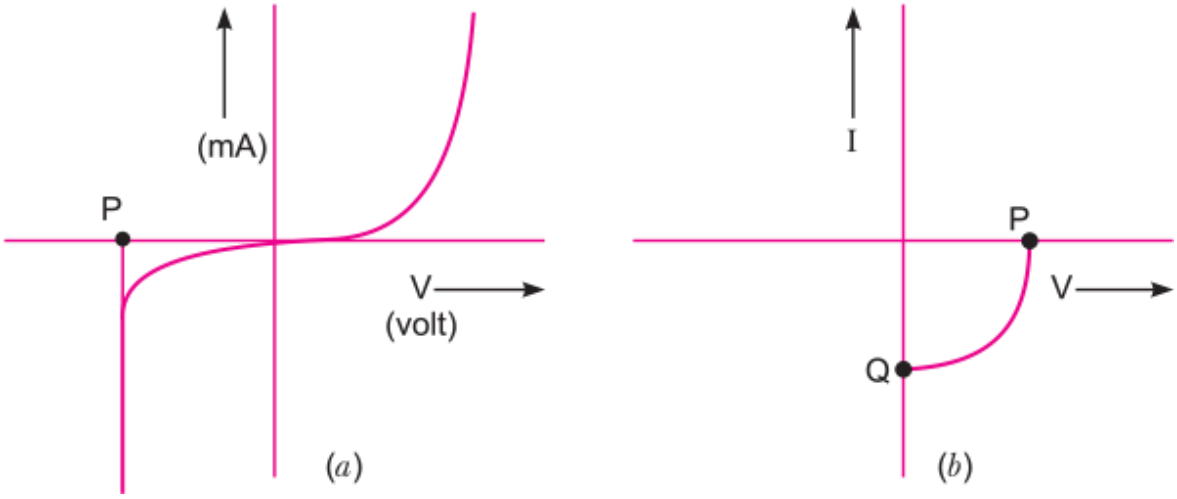
$$\text{b. Voltage gain } A_v = \frac{R_L}{R_i} \times \beta$$

Given RL = 5 kΩ = 5 × 103 Ω,

$$\therefore \quad A_v = \frac{5 \times 10^3}{1000} \times 1000 = 500$$

As CE amplifier causes a phase shift of 180° between input and output voltages, so voltage gain, A_v = – 500.

Q. 7. Answer the following question :



(i) Name the type of a diode whose characteristics are shown in fig (a) and (b).

(ii) What does the points P in fig. (a) represent?

(iii) What does the points P and Q in fig (b) represent?
[HOTS][NCERT Exemplar]

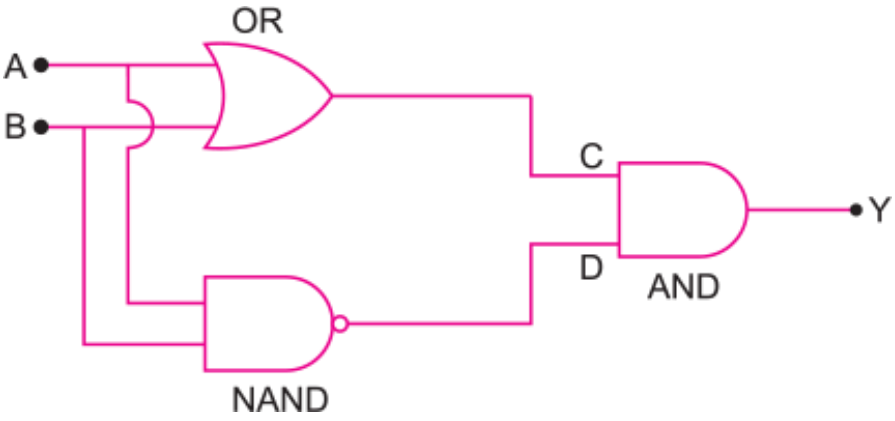
Ans. (i) ZENER junction diode and solar cell.

(ii) Zener breakdown voltage.

(iii) Q-short circuit current

P-open circuit voltage.

Q. 8. Identify the logic gate represented by the following circuit by writing its truth table:



Ans.

The output of OR gate, $C = A + B$

The output of NAND gate, $D = \overline{AB}$

The inputs of *AND* gate are *C* and D, so its output is $Y = C \,.\, D = (A + B)\ \overline{AB}$

When $A = 0, B = 0, Y = (0 + 0)\ \overline{(0 \,.\, 0)} = 0 \,.\, \overline{0} = 0 \,.\, 1 = 0$

When $A = 1, B = 0, Y = (1 + 0)\ \overline{(1 \,.\, 0)} = 1 \,.\, \overline{0} = 1 \,.\, 1 = 1$

When $A = 0, B = 1, Y = (0 + 1)\ \overline{(0 \,.\, 1)} = 1 \,.\, \overline{0} = 1 \,.\, 1 = 1$

When $A = 1, B = 1, Y = (1 + 1)\ \overline{(1 \,.\, 1)} = 1 \,.\, \overline{1} = 1 \,.\, 0 = 0$

Thus, truth table of given circuit is:

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

This is the truth table of XOR gate, hence the given circuit represents **XOR gate.**

Q. 9. Give reasons for the following:

(i) The Zener diode is fabricated by heavily doping both the p and n sides of the junction.

(ii) A photodiode, when used as a detector of optical signals is operated under reverse bias.

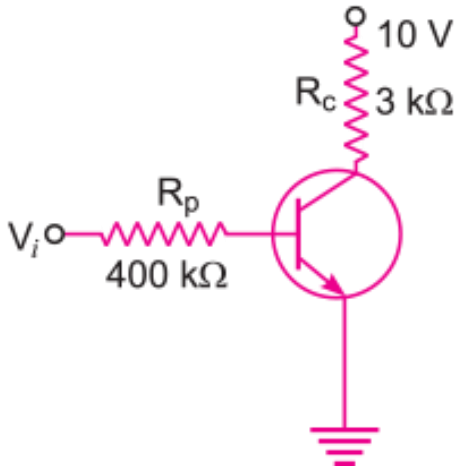
(iii) The band gap of the semiconductor used for fabrication of visible LED's must at least be 1.8 eV. [HOTS]

Ans. (i) Heavy doping makes the depletion region very thin. This makes the electric field of the junction very high, even for a small reverse bias voltage. This in turn helps the Zener diode to act as a 'voltage regulator'.

(ii) When operated under reverse bias, the photodiode can detect changes in current with changes in light intensity more easily.

(iii) The photon energy, of visible light photons varies about 1.8 eV to 3 eV. Hence, for visible LED's, the semiconductor must have a band gap of 1.8 eV.

Q. 10. In the circuit shown in figure, when the input voltage of the base resistance is 10 V, V_{BE} is zero and V_{CE} is also zero. Find the values of I_B, I_C and β. [HOTS][NCERT Exemplar]



Ans.

As $V_{BE} = 0$, potential drop across R_B is 10 V.

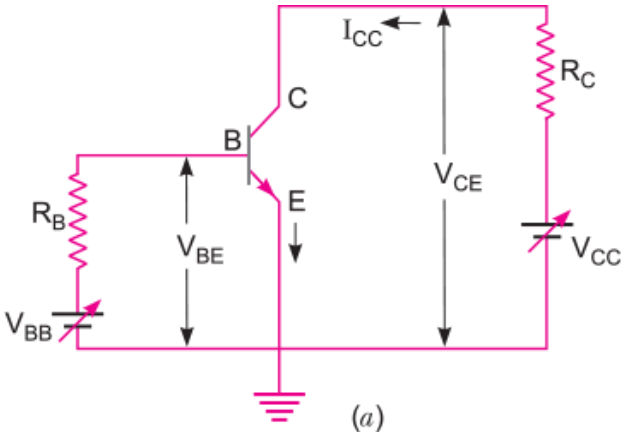
$$\therefore \quad I_B = \frac{10}{400\times10^3} = 25\mu A \qquad (\because V_i - V_{BE} = R_B I_B)$$

Since $V_{CE} = 0$, potential drop across R_C *i.e.*, $I_C R_C$ is 10 V.

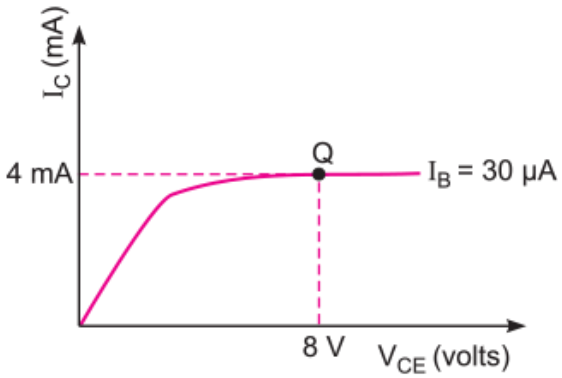
$$\therefore \quad I_C = \frac{10}{3\times10^3} = 3.33\times10^{-3} = 3.33 \text{ mA} \qquad (\because V_{CC} - V_{CE} = I_C R_C)$$

$$\therefore \quad \beta = \frac{I_C}{I_B} = \frac{333\times10^{-3}}{25\times10^{-6}} = 1.33\times10^2 = 133.$$

Q. 11. Consider the circuit arrangement shown in Fig. (a) for studying input and output characteristics of npn transistor in CE configuration. [HOTS]



(a)



(b)

Select the values of R_B and R_C for a transistor whose V_{BE} = 0.7 V, so that the transistor is operating at point Q as shown in the characteristics shown in Fig. (*b*).

Given that the input impedance of the transistor is very small and $V_{CC} = V_{BB}$ = 16V, also find the voltage gain and power gain of circuit making appropriate assumptions.
[*NCERT Exemplar*]

Ans. From the output characteristics at point Q, V_{CE} = 8 V and I_C = 4 mA

$V_{CC} = I_C R_C + V_{CE}$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{16 - 8}{4\times10^{-3}} = 2\,k\Omega$$

$$\text{Since, } V_{BB} = I_B R_B + V_{BE} \quad \text{or} \quad R_B = \frac{V_{BB} - V_{BE}}{I_B} \quad \Rightarrow$$

$$R_B = \frac{16 - 0.7}{30\times10^{-6}} = 510\,k\Omega$$

$$\text{Now, } \beta = \frac{I_C}{I_B} = \frac{4\times10^{-3}}{30\times10^{-6}} = 133$$

$$\text{Voltage gain} = A_v = -\beta\frac{R_C}{R_B} = -133 \times \frac{2\times10^3}{510\times10^3} = -0.52$$

$$\text{Power gain} = A_p = \beta \times A_V = 133 \times 0.52 = 69$$

Q. 12. Explain the following:

(i) In the active state of the transistor, the emitter base junction acts as a low resistance while base collection region acts as high resistance.

(ii) Output characteristics are controlled by the input characteristics in common emitter transistor amplifier.

(iii) LEDs are made of compound semiconductor and not by elemental semiconductors.

[HOTS][CBSE Sample Paper 2016]

Ans. (i) Emitter base junction is forward biased whereas collector base junction is reverse biased.

(ii) Small change in the current I_B in the base circuit controls the large current I_C in the collector circuit $I_C = \beta I_B$

(iii) Elemental semiconductor's band gap is such that the emitted wavelength lies in I_R region. Hence cannot be used for making LED.

Long Answer Questions

Q. 1. (a) State briefly the processes involved in the formation of p-n junction explaining clearly how the depletion region is formed.

(b) Using the necessary circuit diagrams, show how the V–I characteristics of a p-n junction are obtained in

(i) Forward biasing (ii) Reverse biasing How are these characteristics made use of in rectification? [CBSE Delhi 2014]

OR

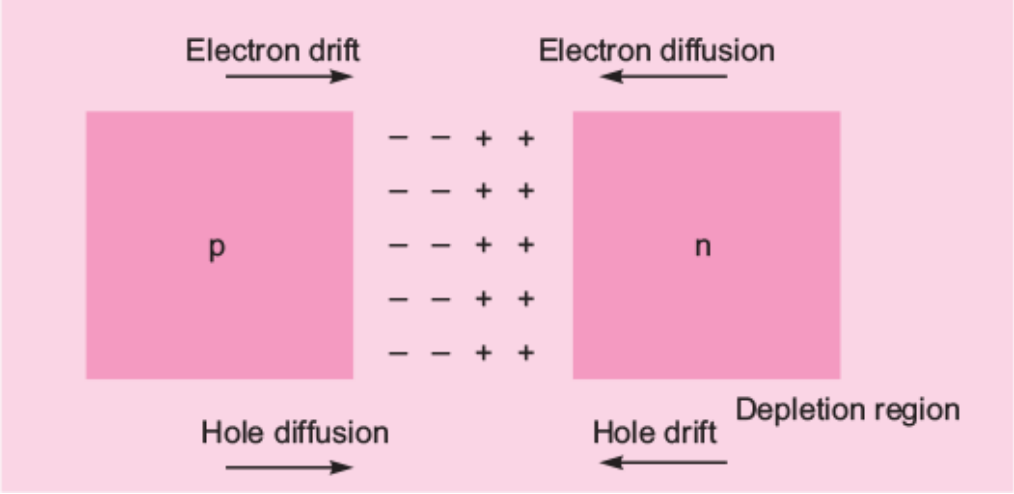
Draw the circuit arrangement for studying the V–I characteristics of a p-n junction diode (i) in forward bias and (ii) in reverse bias. Draw the typical V–I characteristics of a silicon diode.

Describe briefly the following terms:

(i) "Minority carrier injection" in forward bias

(ii) "Breakdown voltage" in reverse bias. [CBSE Chennai 2015]

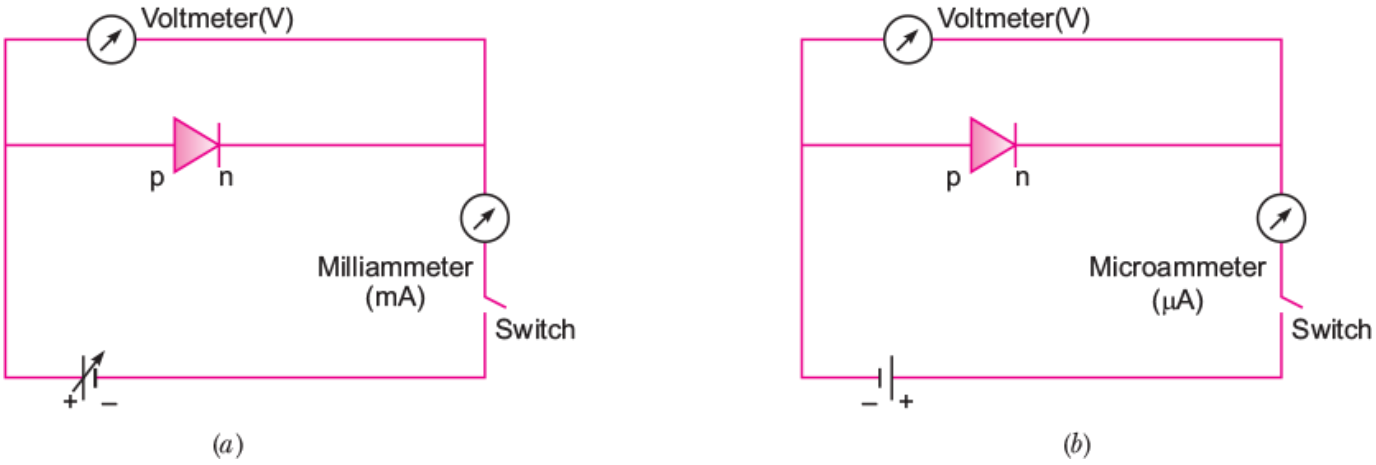
Ans. (a)

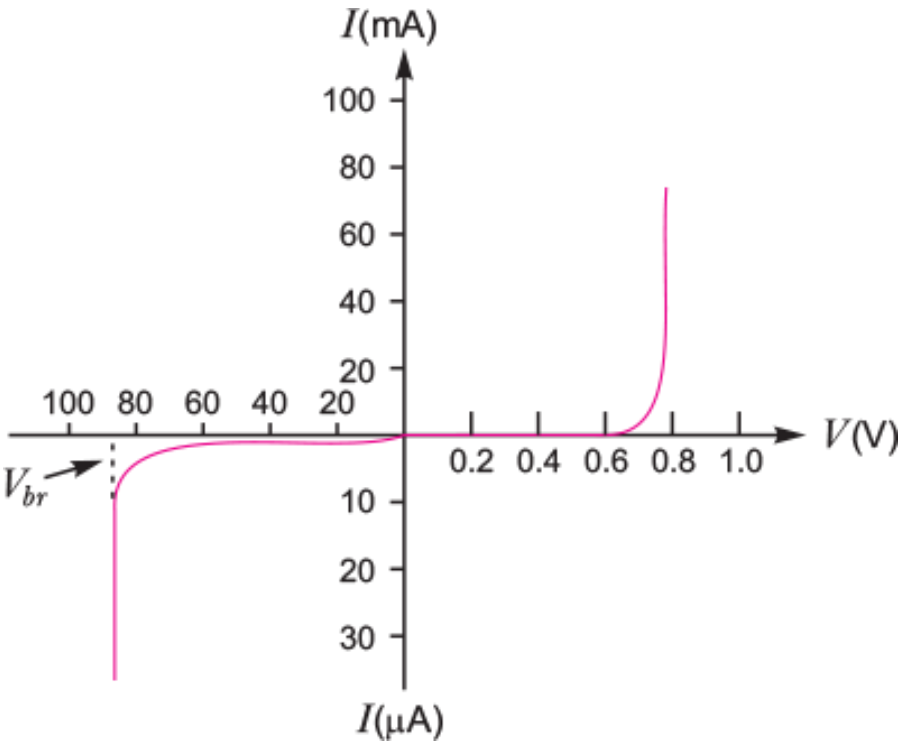


Two processes occur during the formation of a p-n junction are diffusion and drift. Due to the concentration gradient across p and n-sides of the junction, holes diffuse from p-side to n-side (p → n) and electrons diffuse from n-side to p-side (n → p). This movement of charge carriers leaves behind ionised acceptors (negative charge φ-immobile) on the p-side and donors (positive charge immobile) on the n-side of the junction. This space charge region on either side of the junction together is known as depletion region.

(b) The circuit arrangement for studying the V–I characteristics of a diode are shown in Fig. (a) and (b). For different values of voltages the value of current is noted. A graph between V and I is obtained as in Figure (c).

From the V–I characteristic of a junction diode it is clear that it allows current to pass only when it is forward biased. So if an alternating voltage is applied across a diode the current flows only in that part of the cycle when the diode is forward biased. This property is used to rectify alternating voltages.



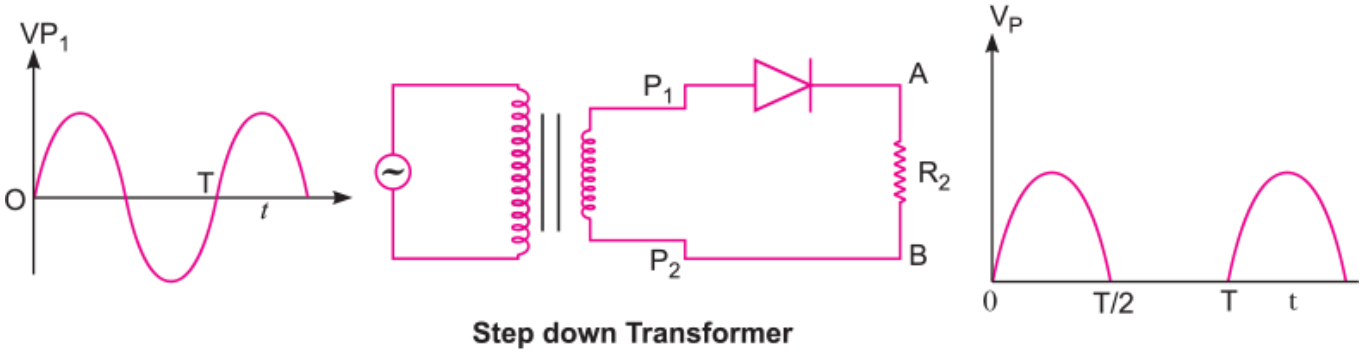


(i) Minority Carrier Injection: Due to the applied voltage, electrons from n-side cross the depletion region and reach p-side (where they are minority carriers). Similarly, holes from p-side cross this junction and reach the n-side (where they are minority carriers). This process under forward bias is known as minority carrier injection.

(ii) Breakdown Voltage: It is a critical reverse bias voltage at which current is independent of applied voltage.

Q. 2. Explain, with the help of a circuit diagram, the working of a p-n junction diode as a half-wave rectifier. [CBSE (AI) 2014]

Ans.



Step down Transformer

Working

(i) During positive half cycle of input alternating voltage, the diode is forward biased and a current flows through the load resistor R_L and we get an output voltage.

(ii) During other negative half cycle of the input alternating voltage, the diode is reverse biased and it does not conduct (under break down region).

Hence, AC voltage can be rectified in the pulsating and unidirectional voltage.

Q. 3. State the principle of working of p-n diode as a rectifier. Explain with the help of a circuit diagram, the use of p-n diode as a full wave rectifier. Draw a sketch of the input and output waveforms. [CBSE Delhi 2012]

OR

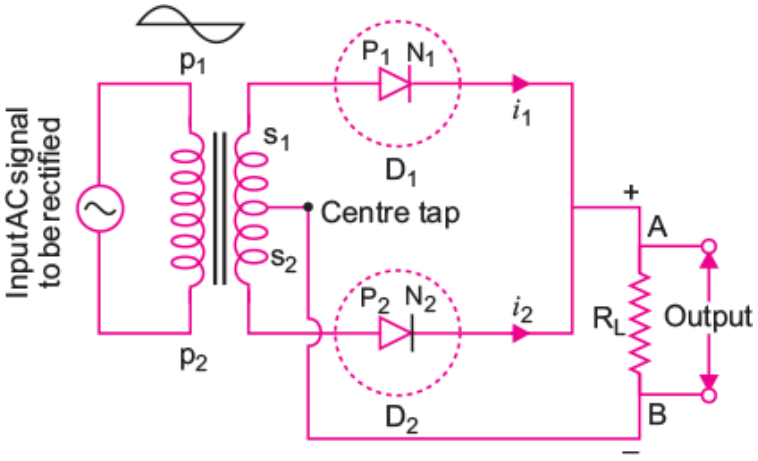
Draw a circuit diagram of a full wave rectifier. Explain the working principle. Draw the input/output waveforms indicating clearly the functions of the two diodes used.
[CBSE (AI) 2011]

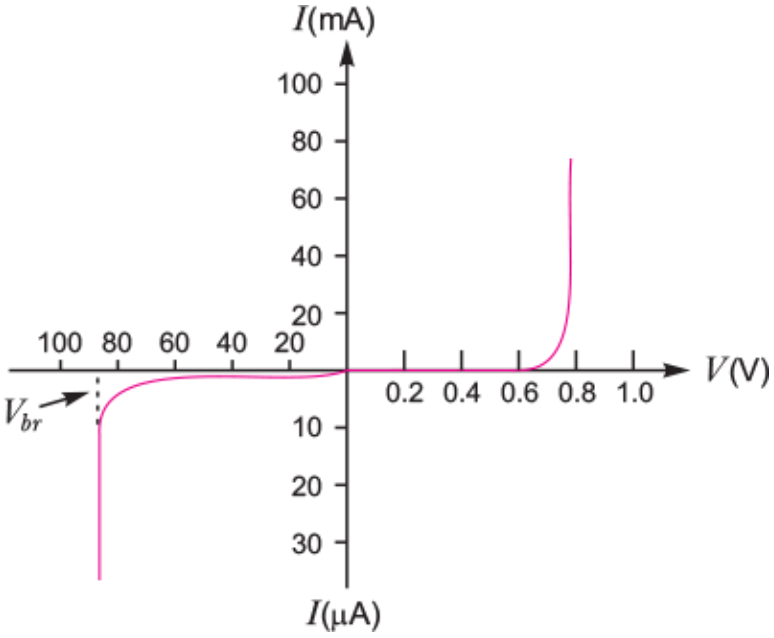
OR

With the help of a circuit diagram, explain the working of a junction diode as a full wave rectifier. Draw its input and output waveforms. Which characteristic property makes the junction diode suitable for rectification?
[CBSE Ajmer 2015, North 2016]

Ans. Rectification: Rectification means conversion of ac into dc. A *p-n* diode acts as a rectifier because an ac changes polarity periodically and a *p-n* diode allows the current to pass only when it is forward biased. This makes the diode suitable for rectification.

Working: The ac input voltage across secondary s_1 and s_2 changes polarity after each half cycle. Suppose during the first half cycle of input ac signal, the terminal s_1 is positive relative to centre tap O and s_2 is negative relative to O. Then diode D_1 is forward biased and diode D_2 is reverse biased. Therefore, diode D_1conducts while diode D_2 does not. The direction of current (i_1) due to diode D_1 in load resistance R_L is directed from A to B In next half cycle, the terminal s_1 is negative and s_2 is positive relative to centre tap O. The diode D_1 is reverse biased and diode D_2 is forward biased. Therefore, diode D_2 conducts while D_1 does not. The direction of current (i_2) due to diode D_2 in load resistance R_L is still from A to B. Thus, the current in load resistance R_L is in the same direction for both half cycles of input ac voltage. Thus *for input ac signal the output current is a continuous series of unidirectional pulses.*





In a full wave rectifier, if input frequency is f hertz, then output frequency will be 2f hertz because for each cycle of input, two positive half cycles of output are obtained.

Q. 4. Answer the following questions.

(i) Explain, how the heavy doping of both p-and n-sides of a p-n junction diode results in the electric field of the junction being extremely high even with a reverse bias voltage of a few volts. [CBSE (F) 2013]

Ans. (i) If p-type and n-type semiconductor are heavily doped. Then due to diffusion of electrons from n-region to p-region, and of holes from p-region to n-region, a depletion region formed of size of order less than 1 μm. The electric field directing from n-region to p-region produces a reverse bias voltage of about 5V and electric field becomes very large.

$$E = \frac{\Delta V}{\Delta x} = \frac{5V}{1\mu m} \approx 5 \times 10^6 V/m$$

Q. 5. Why is a Zener diode considered as a special purpose semiconductor diode?

Draw the I–V characteristic of a zener diode and explain briefly how reverse current suddenly increases at the breakdown voltage.

Describe briefly with the help of a circuit diagram how a Zener diode works to obtain a constant dc voltage from the unregulated dc output of a rectifier. [CBSE (F) 2012]

OR

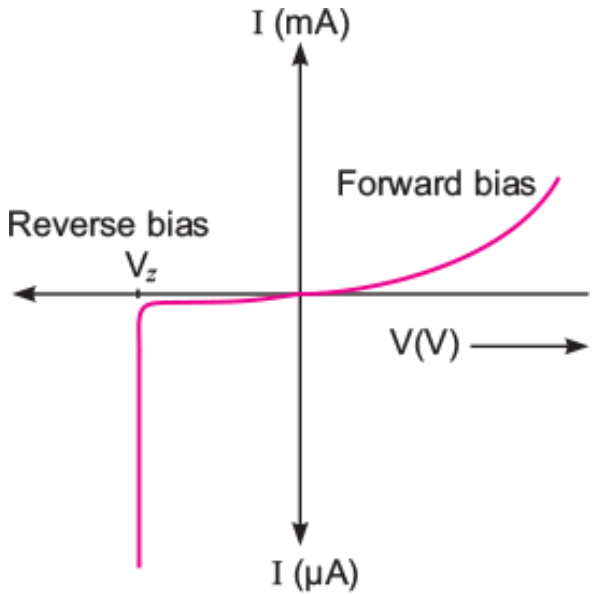
How is Zener diode fabricated? What causes the setting up of high electric field even for small reverse bias voltage across the diode?

Describe with the help of a circuit diagram, the working of Zener diode as a voltage regulator. [CBSE Panchkula 2015]

Ans. A Zener diode is considered as a special purpose semiconductor diode because it is designed to operate under reverse bias in the breakdown region.

Zener diode is fabricated by heavy doping of its p and n sections. Since doping is high, depletion layer becomes very thin.

Hence, electric field $\left(= \frac{v}{l}\right)$ becomes high even for a small reverse bias.

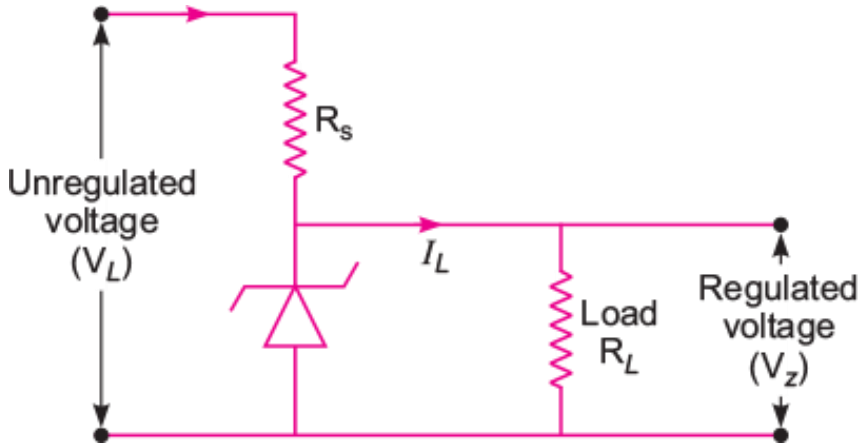


We know that reverse current is due to the flow of electrons (minority carriers) from $p \rightarrow n$ and holes from $n \rightarrow p$. As the reverse bias voltage is increased, the electric field at the junction becomes significant. When the reverse bias voltage $V = V_Z$, then the electric field strength is high enough to pull valence electrons from the host atoms on the *p*-side which are accelerated to *n*-side. These electrons causes high current at breakdown.

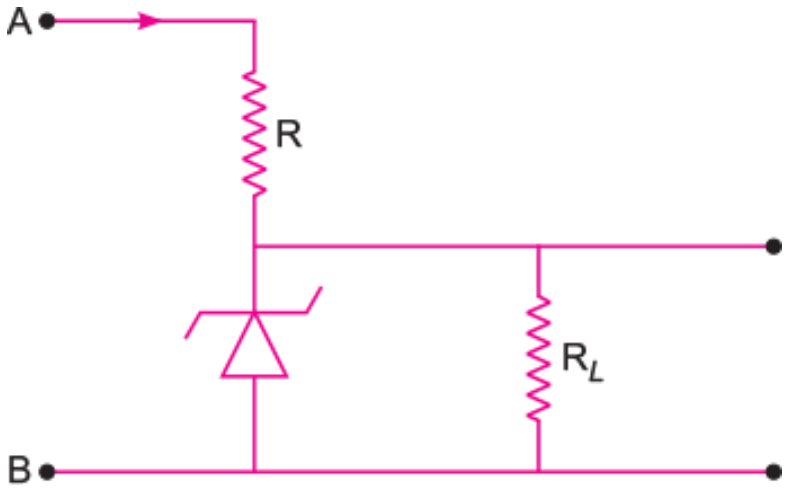
Working:

The unregulated dc voltage output of a rectifier is connected to the zener diode through a series resistance R_s such that the Zener diode is reverse biased. Now, any increase/decrease in the input voltage results in increase/decrease of the voltage drop across R_s without any change in voltage across the Zener diode. Thus, the Zener diode acts as a voltage regulator.

Explanation of voltage regulator.

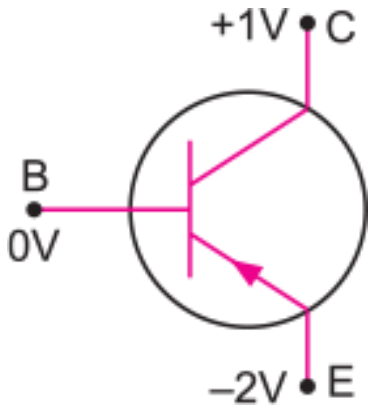


If reverse bias voltage V reaches the breakdown voltage V_Z of zener diode, there is a large change in the current. After that (just above V_Z there is a large change in the current by almost insignificant change in reverse bias voltage. This means diode voltage remains constant.



For example: If unregulated voltage is supplied at terminals A and B, and input voltage increases, the current through resistor R_Z and diode also increases. This current increases the voltage across R_Z without any change in the voltage across diode. Thus, we have a regulated voltage across load resistor R_L.

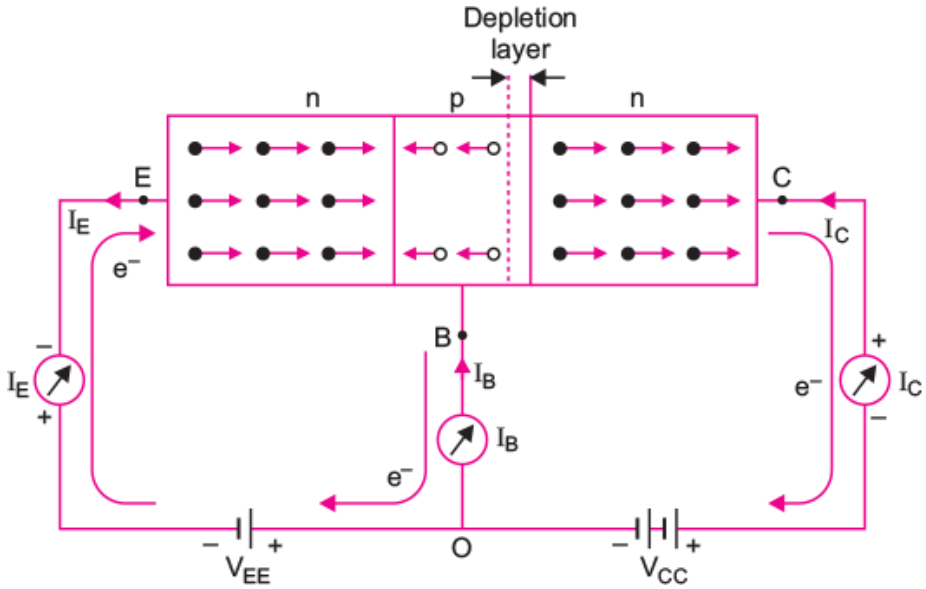
Q. 6. In the figure given alongside, is (i) the emitter and (ii) the collector forward or reverse biased? With the help of a circuit diagram explain the action of npn transistor.
[CBSE (AI) 2012]



Ans. The given transistor is *p-n-p* transistor. The emitter is reverse biased and the collector is forward biased.

Action of *n-p-n* transistor

An *npn* transistor is equivalent to two *p*-*n* junction diodes placed back to back with their very thin *p*-regions connected together. The circuit diagram for the operation of *npn* transistor is shown in fig. The two batteries V_{EE} and V_{CC} represent emitter supply and collector supply respectively.



Transistor Action: Transistor works only when its emitter-base junction is forward biased and collector-emitter junction is reversed biased. Due to this the majority charge carriers from the emitter, accelerate to collector side and create I_E, I_B and I_C such that $I_E = I_B + I_C$.

Base Current and Collector Current: Under forward bias of emitter-base junction, the electrons in emitter and holes in base are compelled to move towards the junction, thus the depletion layer of emitter-base junction is eliminated. As the base region is very thin, most electrons (about 98%) starting from emitter region cross the base region and reach the collector while only a few of them (about 2%) combine with an equal number of holes of base-region and get neutralised. As soon as a hole (in -region) combines with an electron, a covalent bond of crystal atom of base region breaks releasing an electron-hole pair. The electron released is attracted by positive terminal of emitter battery V_{EE}, giving rise to a feeble base current *(I_B).* Its direction in external circuit is from emitter to base. The hole released in the base region compensates the loss of hole neutralised by electrons.

The electrons crossing the base and entering the collector, due to reverse biasing of collector-base junction, are attracted towards the positive terminal of collector battery V_{CC}. In the process an equal number of electrons leave the negative terminal of battery V_{CC} and enter the positive terminal of battery V_{EE}. This causes a current in collector circuit, called the collector current. In addition to this the collector current is also due to flow of minority charge carriers under reverse bias of base-collector junction. This current is called the leakage current.

Thus, collector current is formed of two components:

(i) Current (I_{nc}) due to flow of electrons (majority charge carriers) moving from emitter to collector.

(ii) Leakage current ($I_{leakage}$) due to minority charge carriers, *i.e.*, $I_c = I_{nc} + I_{leakage}$.

Emitter Current: When electrons enter the emitter battery V_{EE} from the base causing base current or electrons enter the collector battery V_{CC} from the collector causing collector current, an equal number of electrons enter from emitter battery V_{EE} to emitter, causing the emitter current. The process continues.

Relation between Emitter, Base and Collector Currents:

Applying Kirchhoff's *I* law at terminal *O*, we get

$I_E = I_B + I_C$

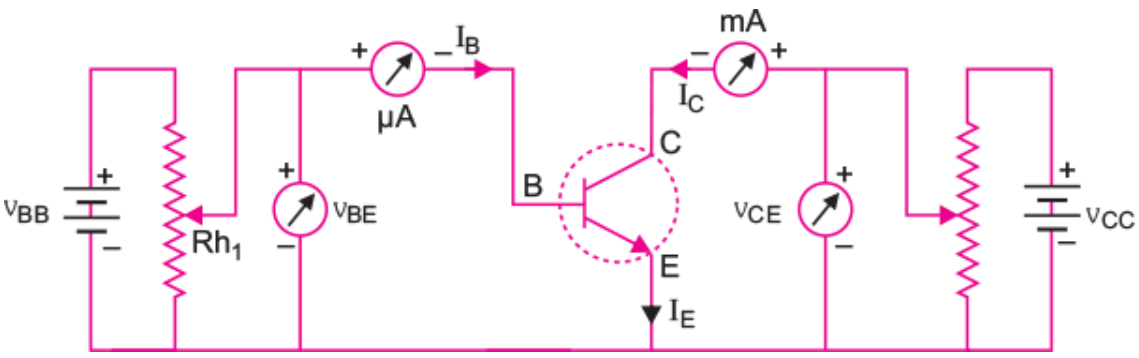
That is, the emitter current I_E is the sum of base current I_B and the collector current I_C. This is the fundamental relation between currents in the bipolar transistor circuit.

Q. 7. Draw the circuit diagram to study the characteristics of npn transistor in common emitter configuration. Sketch typical (i) input characteristics (ii) output characteristics for such a configuration. Explain how the current gain of transistor is calculated from output characteristics. [CBSE Delhi 2009]

OR

Draw the circuit arrangement for studying the input and output characteristics of an n-p-n transistor in CE configuration. With the help of these characteristics define (i) input resistance, (ii) current amplification factor.
[CBSE (AI) 2010; (F) 2013, Delhi 2015]

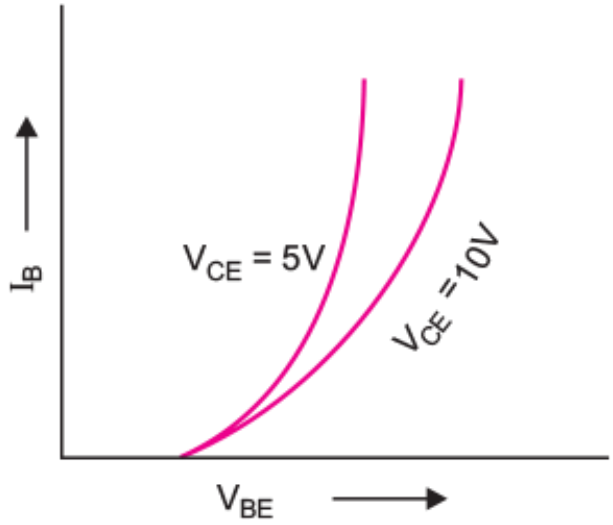
Ans. Characteristic Curves: The circuit diagram for determining the static characteristic curves of an n-p-n transistor in common-emitter configuration is shown in figure.



Common Emitter Characteristics:

(i) Input characteristics are obtained by recording the values of base current I_B for different values of base-emitter voltage V_{BE} at constant collector emitter voltage V_{CE}.

(ii) Output characteristics are obtained by recording the values of collector current I_C for different values of collector emitter voltage V_{CE} at constant base current I_B.



The characteristic curves show:

When collector-emitter voltage V_{CE} is increased from zero, the collector current I_C increases as V_{CE} increases from 0 to 1 V only and then the collector current becomes almost constant and independent of V_{CE}. The value of V_{CE} upto which collector current I_C changes is called the knee voltage V_{knee}

Definition of Input resistance:

Refer to Point 11(*a*) of Basic Concepts.

Definition of Amplification Factor: Refer to Point 12 of Basic Concepts.

Determination of Current Gain

$$\text{Current gain } \beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

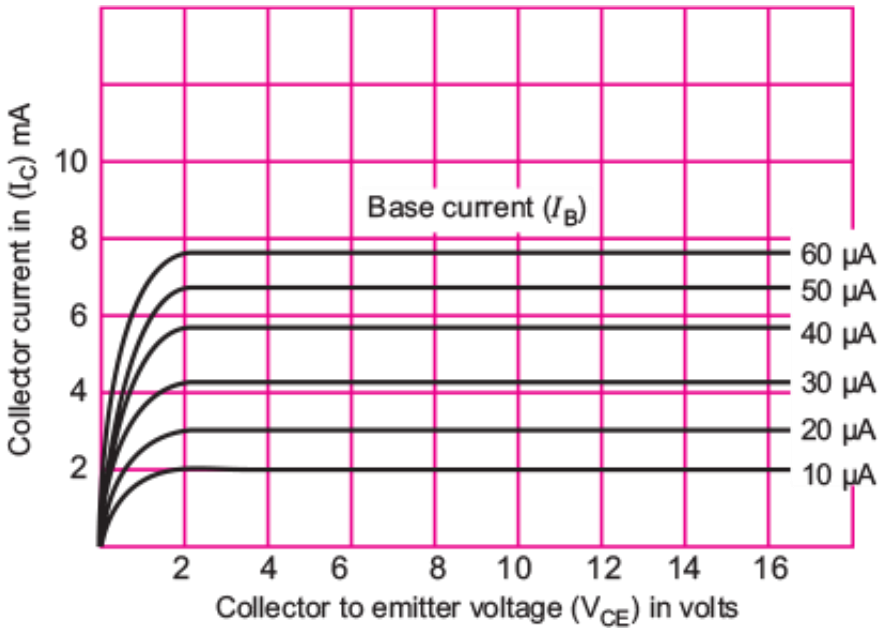
We take the active region of output characteristics *i.e,* the region where collector current (I_C) is almost independent of V_{CE}.

Now we choose any two characteristic curves for given values of I_B and find the two corresponding values of I_C.

Then $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right) = \frac{(I_C)_2 - (I_C)_1}{(I_B)_2 - (I_B)_1}$

From graph $(I_C)_1$ =5.2 mA, $(I_C)_2$ =7.3 mA,

$(I_B)_1$ =30 μA, $(I_B)_2$ = 40 μA



$$\beta = \frac{(7.3 - 5.2)\ \text{mA}}{(40 - 30)\mu A} = \frac{2.1\times10^{-3}}{10\times10^{-6}} = 210$$

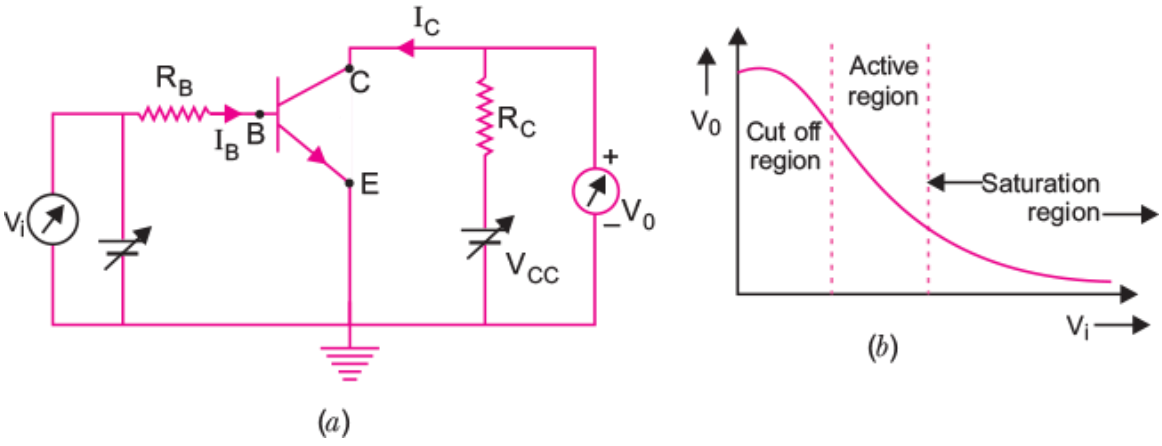
Q. 8. Draw the transfer characteristics of a base biased transistor in common emitter configuration. Explain briefly the meaning of the term active region in these characteristics. For what practical use, do we use the transistor in this active region?

Explain clearly how the active region of the V_0 versus V_i curve in a transistor is used as an amplifier. [CBSE Delhi 2011]

Ans. Transfer characteristics of a base biased transistor in common-emitter configuration:

These are the curves representing the variation of output voltage (V_{BE}) with input voltage (V_{CE})

Circuit Diagram: It is shown in fig. (*a*).



For plotting the curve the input voltage (V_i) is changed in small steps and the corresponding output voltage is measured. The curve obtained is shown in fig. Curve is nearly linear.

In active region the transistor is used as an amplifier.

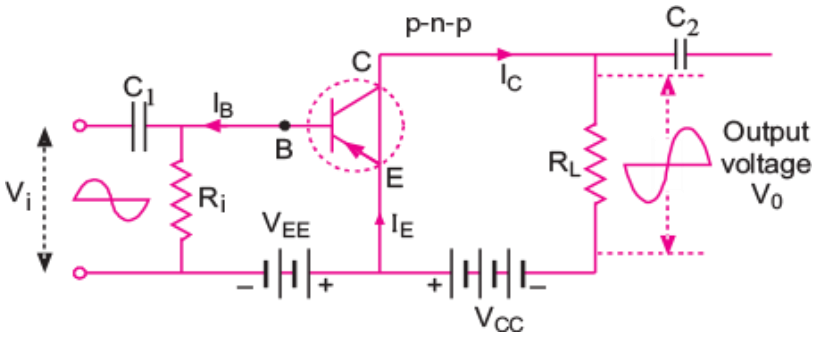
The switching circuits are designed in such a way that the transistor does not remain in active state.

In the active region, a small increase of V_i results in a large (almost linear) increase in I_C. This results in an increase in the voltage drop across R_C.

Q. 9. Draw a labelled circuit diagram of a common emitter amplifier using a p-n-p transistor. Define the term voltage gain and write an expression for it. Explain how the input and output voltages are out of phase by 180° for a common-emitter transistor amplifiers.

Ans. Common-Emitter Transistor Amplifier: Given below is the circuit for a p-n-p transistor. In this circuit, the emitter is common to both the input (emitter-base) and output (collector-emitter) circuits and is grounded. The emitter-base circuit is forward biased and the base-collector circuit is reverse biased.

In a common-emitter circuit, the collector-current is controlled by the base-current rather than the emitter-current. Since in a transistor, when input signal is applied to base, a very small change in base-current provides a much larger change in collector-current and thus extremely large current gains are possible.



When positive half cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease. It decreases the voltage drop across load R_L and thus makes collector voltage more negative. Thus, when input cycle varies through a positive half cycle, the output voltage developed at the collector varies through a negative half cycle and vice versa. Thus, the output voltage in common-emitter amplifier is in antiphase with the input signal or the output and input voltages are 180° out of phase.

Current Gain. The ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) is called the alternating current gain denoted by β Thus,

$$\beta(\text{ ac }) = \frac{\Delta I_C}{\Delta I_B}$$

β has positive values and is generally greater than 20.

Voltage Gain. The voltage gain of common- emitter transistor amplifier is given by

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_L \, \Delta I_C}{R_i \, \Delta \, I_b} = \left(\frac{\Delta I_C}{\Delta I_b}\right) \cdot \frac{R_L}{R_i}$$

$$\Rightarrow \qquad A_v = \beta \frac{R_L}{R_i}$$

Q. 10. (a) Differentiate between three segments of a transistor on the basis of their size and level of doping.

(b) How is a transistor biased to be in active state? [CBSE Delhi 2014]

(c) With the help of necessary circuit diagram describe briefly how npn transistor in CE configuration amplifies a small sinusoidal input voltage. Write the expression for ac current gain.

OR

Explain with the help of a circuit diagram the working of npn transistor as a common emitter amplifier. [CBSE Delhi 2009, South 2016]

OR

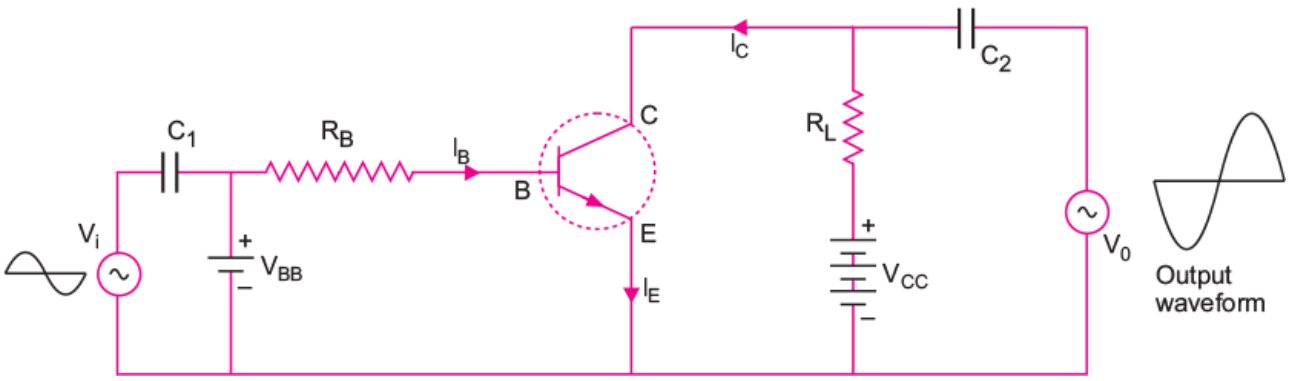
Draw the circuit diagram of a common-emitter amplifier using an npn transistor. What is the phase difference between the input signal and output voltage? Draw the input and output waveforms of the signal. Write the expression for its voltage gain. State two reasons why a common emitter amplifier is preferred to a common base amplifier. [CBSE (AI) 2009, Allahabad 2015]

Ans. (a) Emitter: It is of moderate size and heavily doped.

Base: It is very thin and lightly doped.
Collector: The collector side is moderately doped and larger in size as compared to the emitter.

(b) Transistor is said to be in active state when its emitter-base junction is suitably forward biased and base-collector junction is suitably reverse biased.

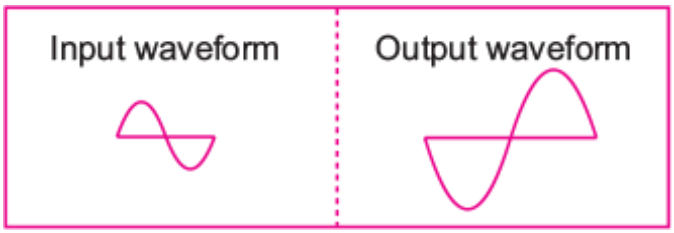
(c) The circuit of common emitter amplifier using n-p-n transistor is shown below:



Working: If a small sinusoidal voltage, with amplitude V_s, is superposed on dc basic bias (by connecting the sinusoidal voltage in series with base supply V_{BB}), the base current will have sinusoidal variations superposed on the base current I_B. As a consequence the collector current is also sinusoidal variations superimposed on the value of collector current I_C, this will produce corresponding amplified changes in the value of output voltage V_0. The ac variations across input and output terminals may be measured by blocking the dc voltage by large capacitors.

The phase difference between input signal and output voltage is 180°.

The input and output waveforms are shown in fig.



Voltage gain $A_v = \beta \frac{R_L}{R_i}$;

ac current gain, $\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$

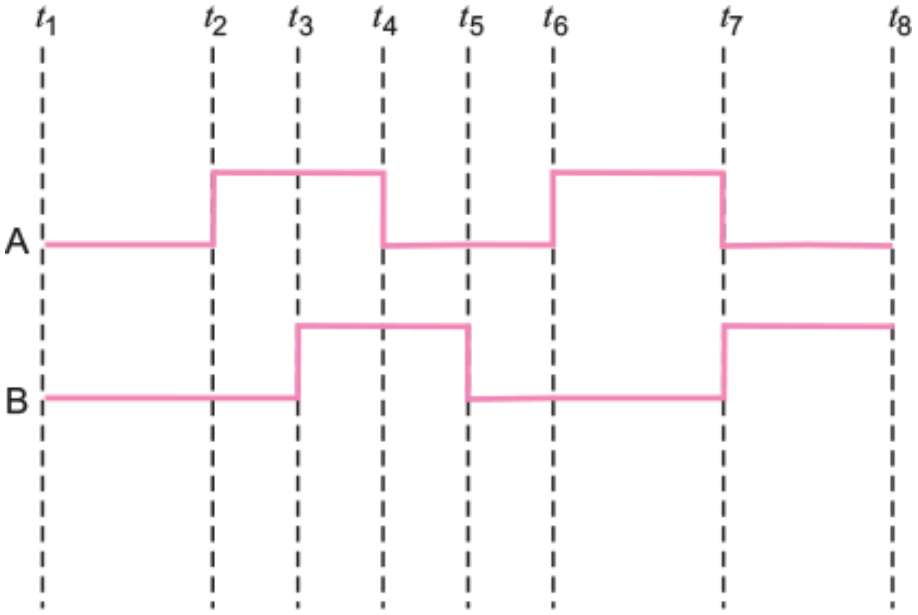
Reasons for using a common emitter amplifier:

(i) Voltage gain is quite high.
(ii) Voltage gain is uniform over a wide frequency range or power gain is high.

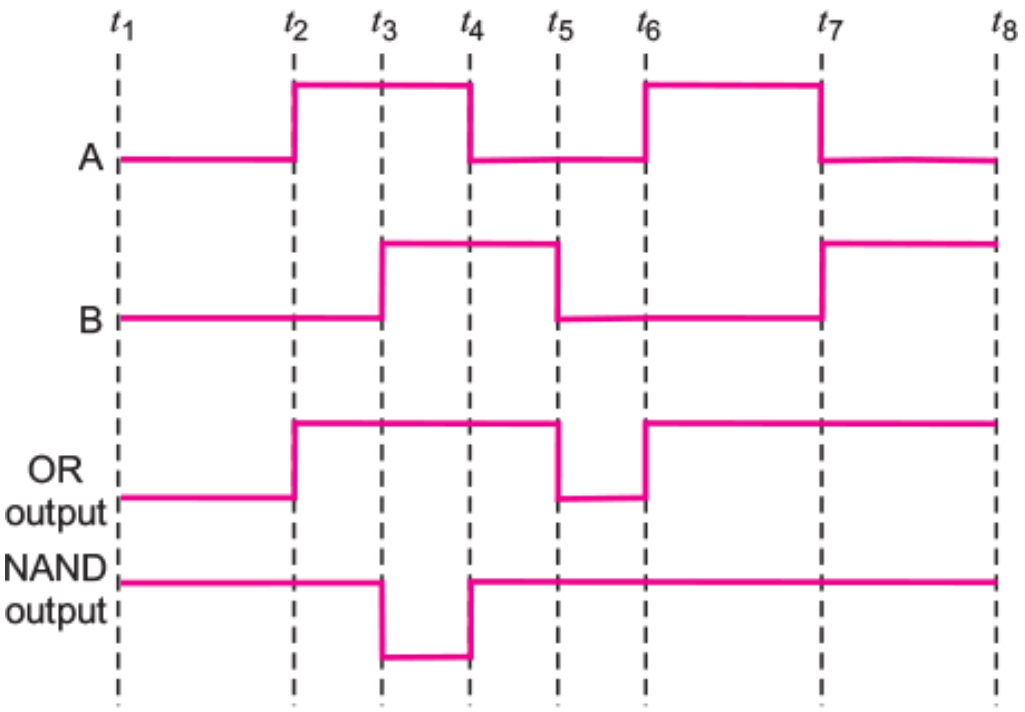
Q. 11. Answer the following questions.

(i) Show the output waveforms (Y) for the following inputs A and B of

(i) OR gate (ii) NAND gate [CBSE Delhi 2012]

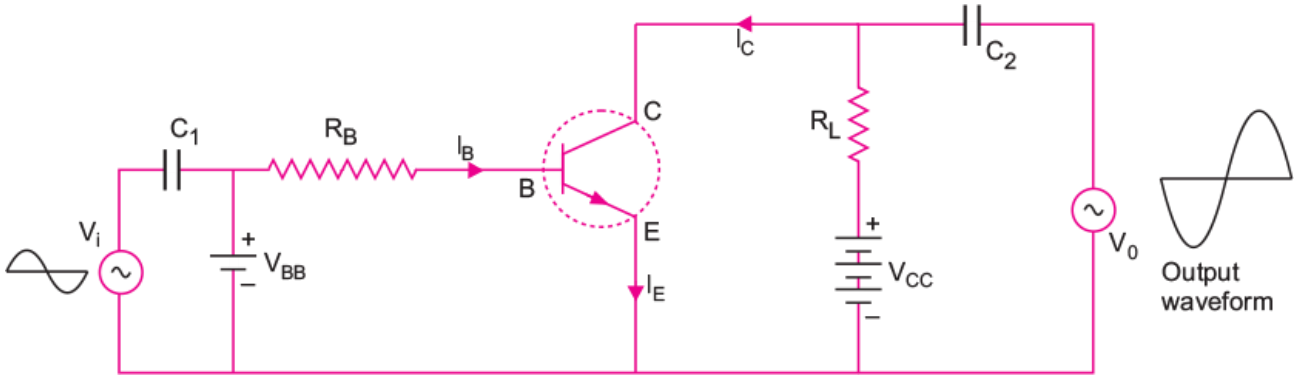


Ans. (i) Output waveforms for the following inputs A and B of OR gate and NAND gate.



Q. 12. Draw a simple circuit of a CE transistor amplifier. Explain its working. Show that the voltage gain AV, of the amplifier is given by $A_V = -\frac{B_{ac} R_L}{r_i}$, where β_{ac} is the current gain, R_L is the load resistance and r_i is the input resistance of the transistor. What is the significance of the negative sign in the expression for the voltage gain?
[CBSE Delhi 2012]

Ans. Circuit diagram of CE transistor Amplifier.



When an ac input signal V_i (to be amplified) is superimposed on the bias V_{BB}, the output, which is measured between collector and ground, increases.

We first assume that $V_i = 0$. Then, applying Kirchhoff's law to the output loop.

$V_{CC} = V_{CE} + I_C R_L$

Similarly, the input loop gives

$V_{BB} = V_{BE} + I_B R_B$

When V_i is not zero, we have

$V_{BE} + V_i = V_{BE} + I_B R_B + \Delta I_B (R_B + R_i)$

$\Rightarrow V_i = \Delta I_B (R_B + R_i) \quad \Rightarrow \quad V_i = r\Delta I_B$

Change in I_B causes a change in I_C

$$\text{Hence, } \beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{I_C}{I_B}$$

$$\text{As } \Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C = 0 \quad \Rightarrow \quad \Delta V_{CE} = -R_L \Delta I_C$$

The change in V_{CE} is the output voltage V_0

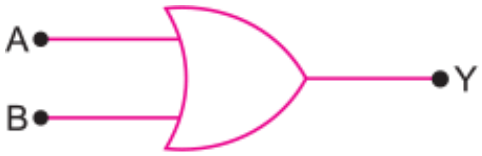
$$\Rightarrow V_0 = R_L \Delta I_C = \beta_{ac} \Delta I_B R_L$$

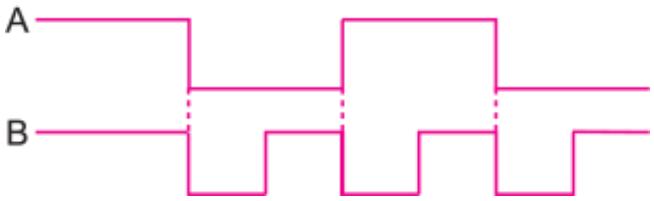
The voltage gain of the amplifier is

$$A_V = \frac{V_0}{V_i} = \frac{\Delta V_{CE}}{r\Delta I_B} = \frac{-\beta_{ac} \Delta I_B R_L}{r\Delta I_B} = -\beta_{ac} \frac{R_L}{r}$$

Negative sign in the expression shows that output voltage and input voltage have phase difference of π.

Q. 13. In fig., the circuit symbol of a logic gate and two input waveforms A and B are shown:





(i) Name the logic gate.
(ii) Write its truth table.
(iii) Give the output waveform.

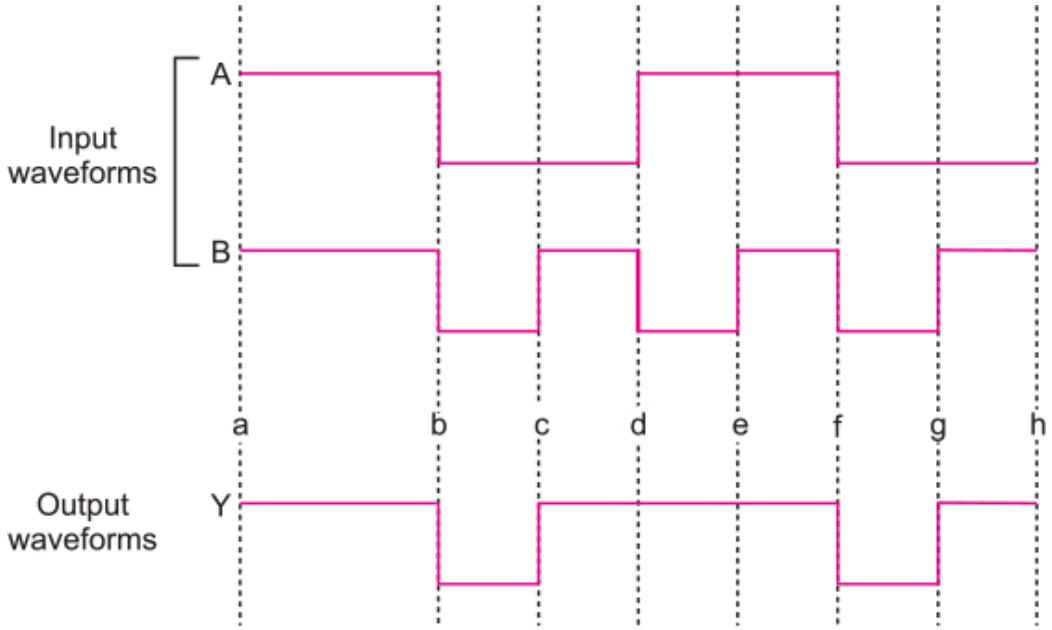
Ans. (i) The logic gate shown is **OR gate.**

(ii) Truth table of OR gate is

Truth table of OR gate is

A	*B*	*Y*
0	0	0
1	0	0
0	1	0
1	1	1

(iii) The input waveforms A and B are discrete square waves. The components of waveforms A and B are shown by vertical dotted lines.



Between *a* and *b, A* = 1, *B* = 1 → Y =1

Between *b* and *c*, *A* = 0, *B* = 0 → Y = 0

Between *c* and *d, A* = 0, *B* = 1 → Y = 1

Between *d* and *e*, *A* =1, *B* = 0 → Y = 1

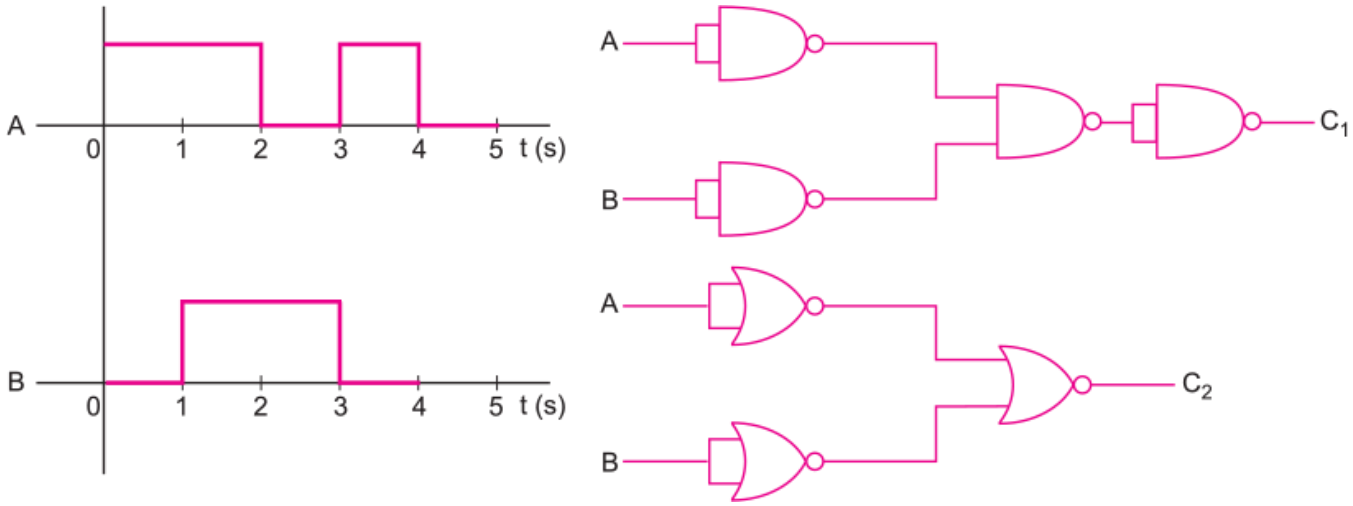
Between *e* and *f*, *A* = 1, *B* = 1 → Y = 1

Between *f* and *g*, *A* = 0, *B* = 0 → Y = 0

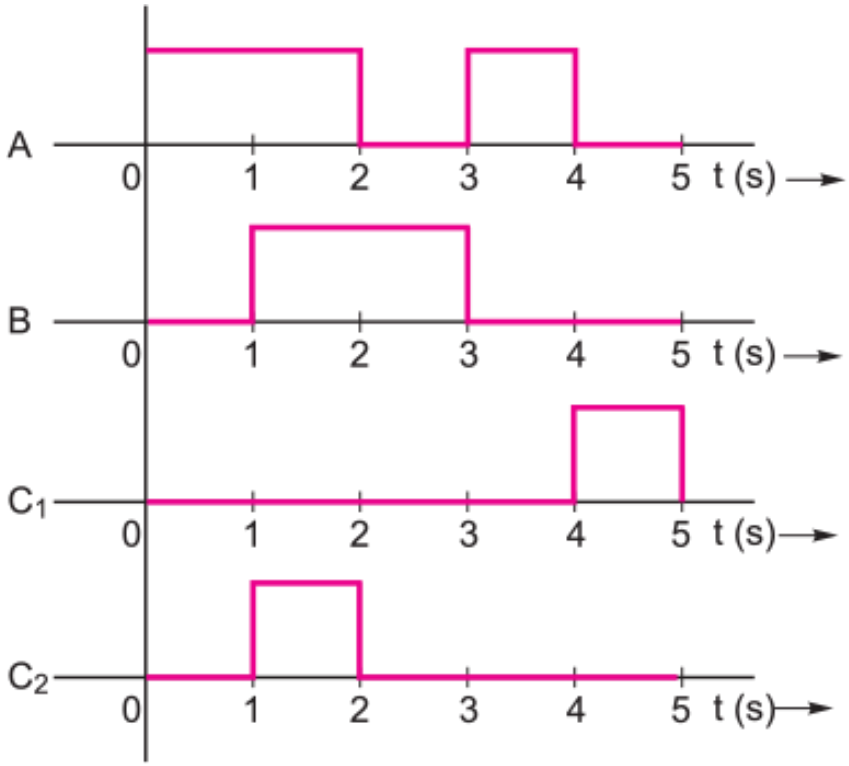
Between *g* and *h*, *A* = 0, *B* = 1 → Y = 1

Accordingly, the waveform *Y* is shown as above.

Q. 14. Draw the output signals C_1 and C_2 in the given combination of gates (Fig.) [HOTS][NCERT Exemplar]



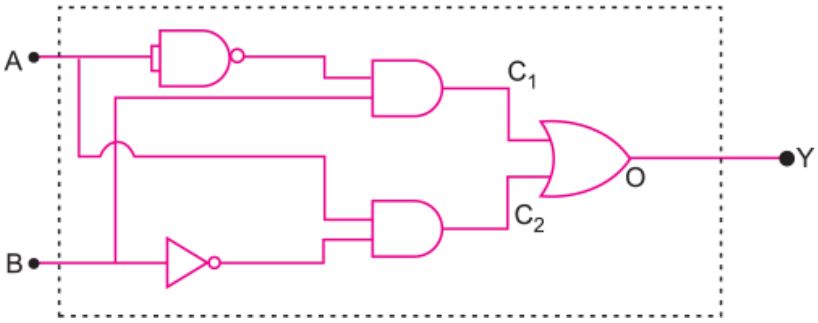
Ans. The output signals C_1 and C_2 are as shown.

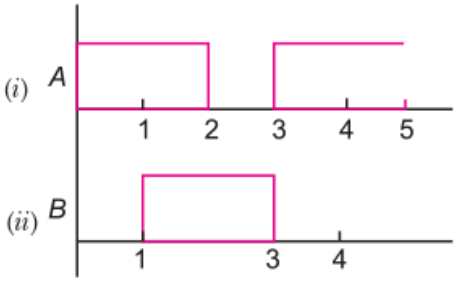


Q. 15. Input signals A and B are applied to the input terminals of the 'dotted box' set-up shown here. Let Y be the final output signal from the box.

Draw the wave forms of the signals labelled as C_1 and C_2 within the box, giving (in brief) the reasons for getting these wave forms. Hence draw the wave form of the final output signal Y. Give reasons for your choice.

What can we state (in words) as the relation between the final output signal Y and the input signals A and B? [HOTS]





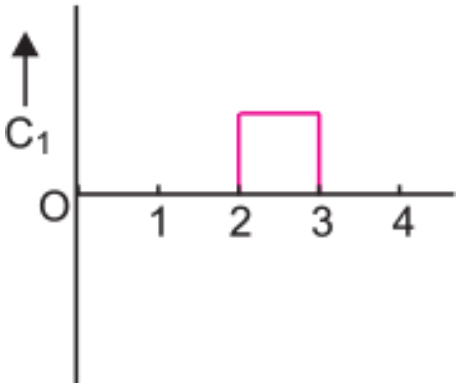
Ans.

$$C_1 = \bar{A}.B, C_2 = A.\bar{B}$$
$$Y = C_1 + C_2 = \bar{A}B + \bar{B}A$$

This is Boolean expression for **NOT XOR gate.**

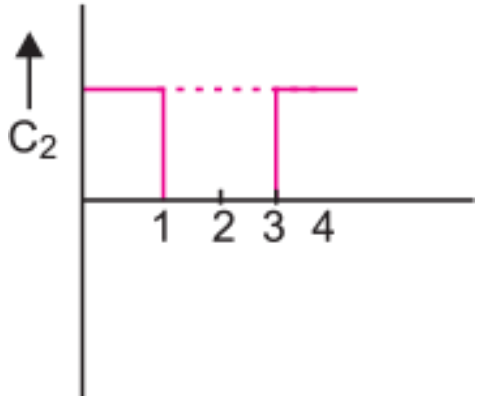
$$C_1 = \bar{A}.B$$

	A	B	$C_1 = \bar{A}.B$
From 0 to 1	1	0	0
From 1 to 2	1	1	0
From 2 to 3	0	1	1
From 3 to 4	1	0	0
From 4 onwards	1	0	0



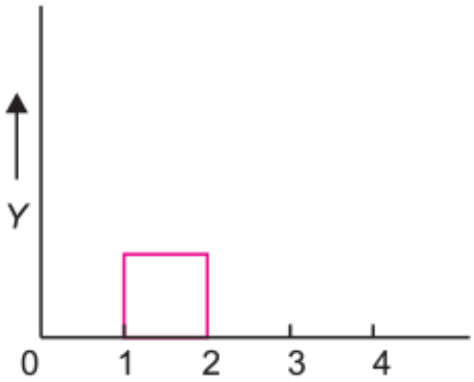
$C_2 = A \cdot \bar{B}$

	A	B	$C_2 = A \cdot \bar{B}$
From 0 to 1	1	0	1
From 1 to 2	1	1	0
From 2 to 3	0	1	0
From 3 to 4	1	0	1
From 4 onwards	1	0	1



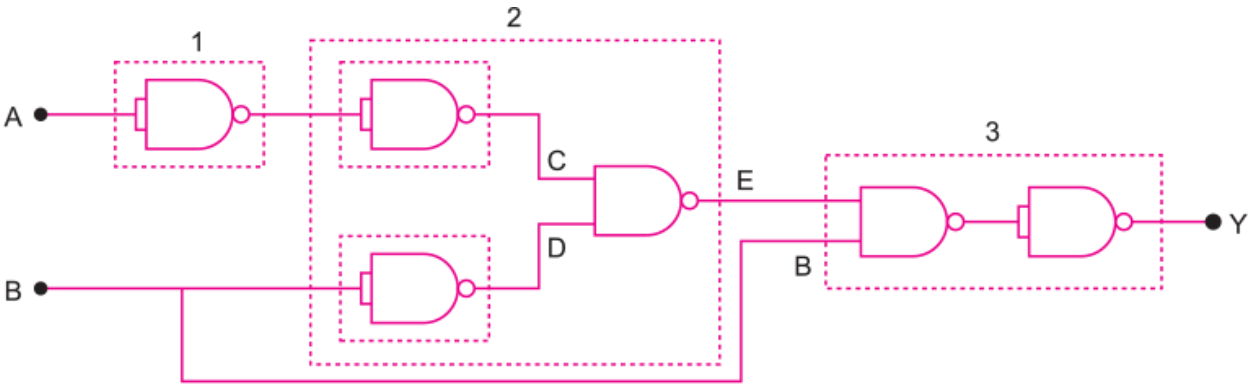
$Y = C_1 \bar{+} C_2$

	A	B	$Y = C_1 \bar{+} C_2$
From 0 to 1	0	1	0
From 1 to 2	0	0	1
From 2 to 3	1	0	0
From 3 to 4	0	1	0
From 4 onwards	0	1	0



The gate shown in circuit is NOT XOR gate. According to definition the output Y is obtained only if either both signals are 0 or 1.

Q. 16. Identify which logic gate OR, AND and NOT is represented by the circuits in the dotted line boxes 1, 2 and 3. Give the truth table for the entire circuit for all possible values of A and B. [HOTS]



Ans. The dotted line box 1 represents NOT gate.

The dotted line box 2 represents OR gate.

The dotted line box 3 represents AND gate.

The output of box 1 is $\bar{A}$

The inputs of box 2 are A and $\bar{B}$

As box 2 is OR gate, therefore, output of box 2 is E = $(\bar{A} + B)$.

The inputs of box 3 are E and B Box 3 represents AND gate; therefore, output of box 3 is

$$Y = EB = (\bar{A} + B)\, B$$

Truth table of the entire circuit is

A	B	$Y = (\bar{A} + B)B$
0	0	$(1 + 0) \cdot 0 = 0$
1	0	$(0 + 0) \cdot 0 = 0$
0	1	$(1 + 1) \cdot 1 = 1 \cdot 1 = 1$
1	1	$(0 + 1) \cdot 1 = 1 \cdot 1 = 1$